ADVANCE INFORMATION

80960CF-40

32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

- *Socket and Object Code Compatible with 80960CA*
- *Two Instructions/Clock Sustained Execution*
- *Four 71 Mbytes/s DMA Channels with Data Chaining*
- *Demultiplexed 32-Bit Burst Bus with Pipelining*

- **32-Bit Parallel Architecture**
  - **Two Instructions/clock Execution**
  - **Load/Store Architecture**
  - **Sixteen 32-Bit Global Registers**
  - **Sixteen 32-Bit Local Registers**
  - **Manipulates 64-Bit Bit Fields**
  - **11 Addressing Modes**
  - **Full Parallel Fault Model**
  - **Supervisor Protection Model**
- **Fast Procedure Call/Return Model**
  - **Full Procedure Call in 4 Clocks**
- **On-Chip Register Cache**
  - **Caches Registers on Call/Ret**
  - **Minimum of 6 Frames Provided**
  - **Up to 15 Programmable Frames**
- **On-Chip Instruction Cache**
  - **4 Kbyte Two-Way Set Associative**
  - **128-Bit Path to Instruction Sequencer**
  - **Cache-Lock Modes**
  - **Cache-Off Mode**
- **High Bandwidth On-Chip Data RAM**
  - **1 Kbyte On-Chip Data RAM**
  - **Sustains 128 bits per Clock Access**
- **Selectable Big or Little Endian Byte Ordering**
- **Four On-Chip DMA Channels**
  - **71 Mbytes/s Fly-by Transfers**
  - **40 Mbytes/s Two-Cycle Transfers**
  - **Data Chaining**
  - **Data Packing/Unpacking**
  - **Programmable Priority Method**
- **32-Bit Demultiplexed Burst Bus**
  - **128-Bit Internal Data Paths to *and* from Registers**
  - **Burst Bus for DRAM Interfacing**
  - **Address Pipelining Option**
  - **Fully Programmable Wait States**
  - **Supports 8-, 16- or 32-Bit Bus Widths**
  - **Supports Unaligned Accesses**
  - **Supervisor Protection Pin**
- **High-Speed Interrupt Controller**
  - **Up to 248 External Interrupts**
  - **32 Fully Programmable Priorities**
  - **Multi-mode 8-Bit Interrupt Port**
  - **Four Internal DMA Interrupts**
  - **Separate, Non-maskable Interrupt Pin**
  - **Context Switch in 625 ns Typical**
- **On-Chip Data Cache**
  - **1 Kbyte Direct-Mapped, Write Through**
  - **128 bits per Clock Access on Cache Hit**

 March 1994 **Order Number: 272493-001**

80960CF-40

32-BIT HIGH-PERFORMANCE SUPERSCALAR PROCESSOR

FIGURES

TABLES

1.0 PURPOSE

This document provides electrical characteristics of Intel's i960® CF embedded 40 MHz microprocessor (also available in 33, 25 and 16 MHz). For descriptions of any 80960CF functional topic — other than parametric performance — consult the *i960® Cx Microprocessor User's Manual* (#270710). To obtain data sheet updates and errata, call Intel's FaxBack data-on-demand system (1-800-628-2283 or 916-356-3105). Other information can be obtained from Intel's technical BBS (916-356-3600).

2.0 80960CF OVERVIEW

Intel's 80960CF is the performance follow-on product to the 80960CA. The 80960CF is socket- and object code-compatible with the CA; this makes CA-to-CF design upgrades straightforward.

As shown in Figure 1, the 80960CF's instruction cache is 4 Kbytes; data cache is 1 Kbyte (80960CA instruction cache is 1 Kbyte; it does not have a data cache.) This extra cache on the CF adds a significant performance boost over the CA.

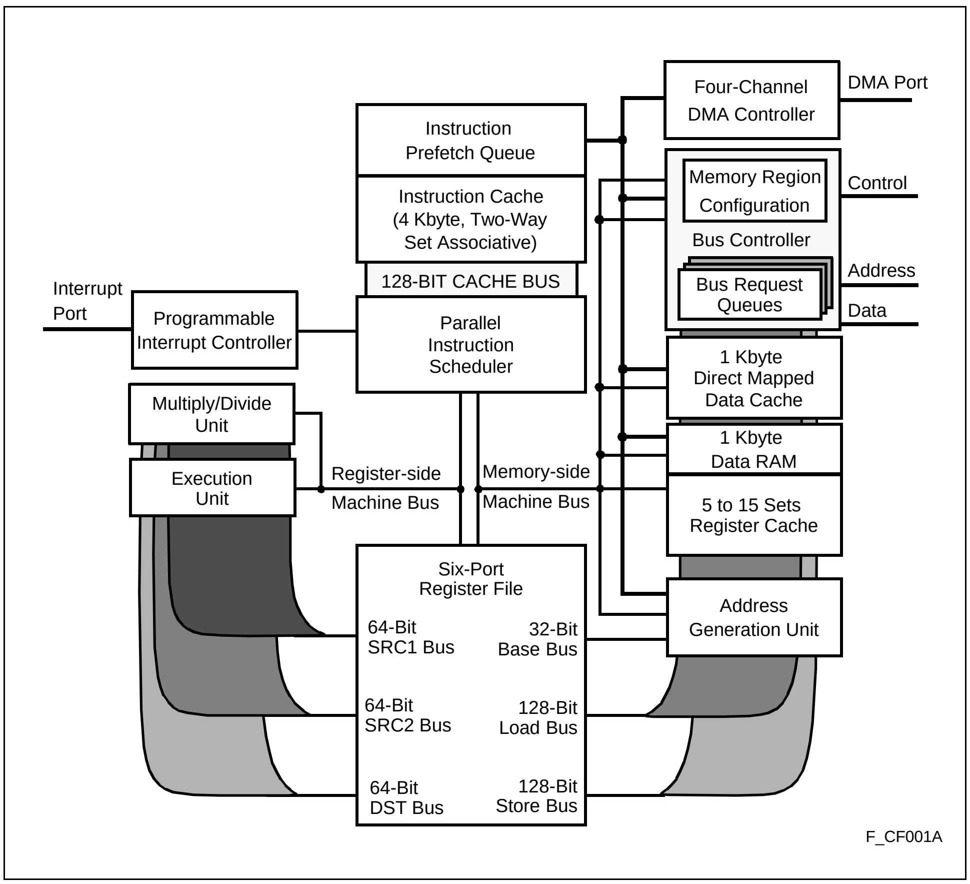


Figure 1. 80960CF Block Diagram

The 80960CF is object code compatible with the 32-bit 80960 Core Architecture while including Special Function Register extensions to control on-chip peripherals and instruction set extensions to shift 64-bit operands and configure on-chip hardware. Multiple 128-bit internal buses, on-chip instruction caching and a sophisticated instruction scheduler allow the processor to sustain execution of two instructions every clock and peak at execution of three instructions per clock.

A 32-bit demultiplexed and pipelined burst bus provides a 160 Mbyte/s bandwidth to a system's high-speed external memory subsystem. Also, the 80960CF's on-chip caching of instructions, procedure context and critical program data substantially decouple system performance from the wait states associated with accesses to the system's slower, cost sensitive, main memory subsystem.

The 80960CF bus controller integrates full wait state and bus width control for highest system performance with minimal system design complexity. Unaligned access and Big Endian byte order support reduces the cost of porting existing applications to the 80960CF.

The processor also integrates four complete data-chaining DMA channels and a high-speed interrupt controller on-chip. DMA channels perform single-cycle or two-cycle transfers, data packing and unpacking and data chaining. Block transfers — in addition to source or destination synchronized transfers — are provided.

The interrupt controller provides full programmability of 248 interrupt sources into 32 priority levels with a typical interrupt task switch (latency) time of 625 ns.

2.1 The C-Series Core

The C-Series core is a very high performance microarchitectural implementation of the 80960 Core Architecture. This core can sustain execution of two instructions per clock (80 MIPS at 40 MHz). To achieve this level of performance, Intel has incorporated state-of-the-art silicon technology and innovative microarchitectural constructs into the C-Series core implementation. Factors that contribute to the core's performance include:

- Parallel instruction decoding allows issuance of up to three instructions per clock
- Single-clock execution of most instructions
- Parallel instruction decode allows sustained, simultaneous execution of two single-clock instructions every clock cycle
- Efficient instruction pipeline minimizes pipeline break losses
- Register and resource scoreboarding allow simultaneous multi-clock instruction execution
- Branch look-ahead and prediction allows many branches to execute with no pipeline break
- Local Register Cache integrated on-chip caches Call/Return context
- Two-way set associative, 4 Kbyte integrated instruction cache
- 1 Kbyte integrated Data RAM sustains a four-word (128-bit) access every clock cycle
- Direct mapped, 1 Kbyte data cache, write through, write allocate

2.2 Pipelined, Burst Bus

A 32-bit high performance bus controller interfaces the 80960CF to external memory and peripherals. The Bus Control Unit features a maximum transfer rate of 160 Mbytes per second (at 40 MHz). Internally programmable wait states and 16 separately configurable memory regions allow the processor to interface with a variety of memory subsystems with a minimum of system complexity and a maximum of performance. The Bus Controller's main features include:

- Demultiplexed, Burst Bus to exploit most efficient DRAM access modes
- Address Pipelining to reduce memory cost while maintaining performance
- 32-, 16- and 8-bit modes for I/O interfacing ease
- Full internal wait state generation to reduce system cost
- Little and Big Endian support to ease application development
- Unaligned access support for code portability
- Three-deep request queue to decouple the bus from the core

2.3 Instruction Set Summary

Table 1 summarizes the 80960CF instruction set by logical groupings. See the *i960® Cx Microprocessor User's Manual* (#270710) for a complete description of the instruction set.

2.4 Flexible DMA Controller

A four-channel DMA controller provides high speed DMA control for data transfers involving peripherals and memory. The DMA provides advanced features such as data chaining, byte assembly and disassembly and a high performance fly-by mode capable of transfer speeds of up to 71 Mbytes per second at 40 MHz. The DMA controller features a performance and flexibility which is only possible by integrating the DMA controller and the 80960CF core.

2.5 Priority Interrupt Controller

A programmable-priority interrupt controller manages up to 248 external sources through the 8-bit external interrupt port. The Interrupt Unit also handles the four internal sources from the DMA controller and a single non-maskable interrupt input. The 8-bit interrupt port can also be configured to provide individual interrupt sources that are level or edge triggered.

80960CF interrupts are prioritized and signaled within 225 ns of the request. If the interrupt is of higher priority than the processor priority, the context switch to the interrupt routine typically completes in another 400 ns. The interrupt unit provides the mechanism for the low latency and high throughput interrupt service which is essential for embedded applications.

Table 1. 80960CF Instruction Set

Data Movement	Arithmetic	Logical	Bit / Bit Field / Byte
Load Store Move Load Address	Add Subtract Multiply Divide Remainder Modulo Shift *Extended Shift Extended Multiply Extended Divide Add with Carry Subtract with Carry Rotate	And Not And And Not Or Exclusive Or Not Or Or Not Nor Exclusive Nor Not Nand	Set Bit Clear Bit Not Bit Alter Bit Scan For Bit Span Over Bit Extract Modify Scan Byte for Equal
Comparison	**Branch**	**Call/Return**	**Fault**
Compare Conditional Compare Compare and Increment Compare and Decrement Test Condition Code Check Bit	Unconditional Branch Conditional Branch Compare and Branch	Call Call Extended Call System Return Branch and Link	Conditional Fault Synchronize Faults
Debug	**Processor Mgmt**	**Atomic**	
Modify Trace Controls Mark Force Mark	Flush Local Registers Modify Arithmetic Controls Modify Process Controls *System Control *DMA Control	Atomic Add Atomic Modify	

NOTES: Instructions marked by (*) are 80960Cx extensions to the 80960 instruction set.

3.0 PACKAGE INFORMATION

3.1 Package Introduction

This section describes the pins, pinouts and thermal characteristics for the 80960CF in the 168-pin Ceramic Pin Grid Array (PGA) package. For complete package specifications and information, see the *Packaging* Handbook (# 240800).

3.2 Pin Descriptions

This section defines the 80960CF pins. Table 2 presents the legend for interpreting the pin descriptions in the following tables. Pins associated with the 32-bit demultiplexed processor bus are described in Table 3. Pins associated with basic processor configuration and control are described in Table 4. Pins associated with the 80960CF DMA Controller and Interrupt Unit are described in Table 5.

All pins float while the processor is in the ONCE mode.

Table 2. Pin Description Nomenclature

Symbol	Description
I	Input only pin
O	Output only pin
I/O	Pin can be either an input or output
–	Pins "must be" connected as described
S(...)	Synchronous. Inputs must meet setup and hold times relative to PCLK2:1 for proper operation. Outputs are synchronous to PCLK2:1. S(E) Edge sensitive input S(L) Level sensitive input
A(...)	Asynchronous. Inputs may be asynchronous to PCLK2:1. A(E) Edge sensitive input A(L) Level sensitive input
H(...)	While the bus is in the Hold Acknowledge or Bus Backoff state, the pin: H(1) is driven to V_{CC} H(0) is driven to V_{SS} H(Z) floats H(Q) continues to be a valid input
R(...)	While the processor's $\overline{RESET}$ pin is low, the pin: R(1) is driven to V_{CC} R(0) is driven to V_{SS} R(Z) floats R(Q) continues to be a valid output

Table 3. 80960CF Pin Description — External Bus Signals (Sheet 1 of 3)

Name	Type	Description
A31:2	**O** S H(Z) R(Z)	**ADDRESS BUS** carries the physical address' upper 30 bits. A31 is the most significant bit; A2 is least significant. During a bus access, A31:2 identify all external addresses to word (4-byte) boundaries. Byte enable signals indicate the selected byte in each word. During burst accesses, A3:2 increment to indicate successive data cycles.
D31:0	**I/O** S(L) H(Z) R(Z)	**DATA BUS** carries 32-, 16- or 8-bit data quantities depending on bus width configuration. The least significant bit is carried on D0 and the most significant on D31. When the bus is configured for 8-bit data, the lower 8 data lines, D7:0 are used. For 16-bit data bus widths, D15:0 are used. For 32-bit bus widths the full data bus is used.
$\overline{BE3:0}$	**O** S H(Z) R(1)	**BYTE ENABLES** select which of the four bytes addressed by A31:2 are active during an access to a memory region configured for a 32-bit data-bus width. $\overline{BE3}$ applies to D31:24; $\overline{BE2}$ applies to D23:16; $\overline{BE1}$ applies to D15:8 $\overline{BE0}$ applies to D7:0. 32-bit bus: $\overline{BE3}$ –Byte Enable 3 –enable D31:24 $\overline{BE2}$ –Byte Enable 2 –enable D23:16 $\overline{BE1}$ –Byte Enable 1 –enable D15:8 $\overline{BE0}$ –Byte Enable 0 –enable D7:0 For accesses to a memory region configured for a 16-bit data-bus width, the processor uses the $\overline{BE3}$, $\overline{BE1}$ and $\overline{BE0}$ pins as $\overline{BHE}$, A1 and $\overline{BLE}$ respectively. 16-bit bus: $\overline{BE3}$ –Byte High Enable ($\overline{BHE}$) –enable D15:8 $\overline{BE2}$ –Not used (driven high or low) $\overline{BE1}$ –Address Bit 1 (A1) $\overline{BE0}$ –Byte Low Enable ($\overline{BLE}$) –enable D7:0 For accesses to a memory region configured for an 8-bit data-bus width, the processor uses the $\overline{BE1}$ and $\overline{BE0}$ pins as A1 and A0 respectively. 8-bit bus: $\overline{BE3}$ –Not used (driven high or low) $\overline{BE2}$ –Not used (driven high or low) $\overline{BE1}$ –Address Bit 1 (A1) $\overline{BE0}$ –Address Bit 0 (A0)
W/$\overline{R}$	**O** S H(Z) R(0)	**WRITE/READ** is asserted for read requests and deasserted for write requests. The W/$\overline{R}$ signal changes in the same clock cycle as $\overline{ADS}$. It remains valid for the entire access in non-pipelined regions. In pipelined regions, W/$\overline{R}$ is not guaranteed to be valid in the last cycle of a read access.
$\overline{ADS}$	**O** S H(Z) R(1)	**ADDRESS STROBE** indicates a valid address and the start of a new bus access. $\overline{ADS}$ is asserted for the first clock of a bus access.
$\overline{READY}$	**I** S(L) H(Z) R(Z)	**READY** is an input which signals the termination of a data transfer. $\overline{READY}$ is used to indicate that read data on the bus is valid or that a write-data transfer has completed. The $\overline{READY}$ signal works in conjunction with the internally programmed wait-state generator. If $\overline{READY}$ is enabled in a region, the pin is sampled after the programmed number of wait-states has expired. If the $\overline{READY}$ pin is deasserted, wait states continue to be inserted until $\overline{READY}$ becomes asserted. This is true for the N_{RAD}, N_{RDD}, N_{WAD} and N_{WDD} wait states. The N_{XDA} wait states cannot be extended.

Table 3. 80960CF Pin Description — External Bus Signals (Sheet 2 of 3)

Name	Type	Description
BTERM	**I** S(L) H(Z) R(Z)	**BURST TERMINATE** is an input which breaks up a burst access and causes another address cycle to occur. The BTERM signal works in conjunction with the internally programmed wait-state generator. If READY and BTERM are enabled in a region, the BTERM pin is sampled after the programmed number of wait states has expired. When BTERM is asserted, a new ADS signal is generated and the access is completed. The READY input is ignored when BTERM is asserted. BTERM must be externally synchronized to satisfy BTERM setup and hold times.
WAIT	**O** S H(Z) R(1)	**WAIT** indicates internal wait state generator status. WAIT is asserted when wait states are being caused by the internal wait state generator and not by the READY or BTERM inputs. WAIT can be used to derive a write-data strobe. WAIT can also be thought of as a READY output that the processor provides when it is inserting wait states.
BLAST	**O** S H(Z) R(0)	**BURST LAST** indicates the last transfer in a bus access. BLAST is asserted in the last data transfer of burst and non-burst accesses after the wait state counter reaches zero. BLAST remains asserted until the clock following the last cycle of the last data transfer of a bus access. If the READY or BTERM input is used to extend wait states, the BLAST signal remains asserted until READY or BTERM terminates the access.
DT/R	**O** S H(Z) R(0)	**DATA TRANSMIT/RECEIVE** indicates direction for data transceivers. DT/R is used in conjunction with DEN to provide control for data transceivers attached to the external bus. When DT/R is asserted, the signal indicates that the processor receives data. Conversely, when deasserted, the processor sends data. DT/R changes only while DEN is high.
DEN	**O** S H(Z) R(1)	**DATA ENABLE** indicates data cycles in a bus request. DEN is asserted at the start of the bus request first data cycle and is deasserted at the end of the last data cycle. DEN is used in conjunction with DT/R to provide control for data transceivers attached to the external bus. DEN remains asserted for sequential reads from pipelined memory regions. DEN is deasserted when DT/R changes.
LOCK	**O** S H(Z) R(1)	**BUS LOCK** indicates that an atomic read-modify-write operation is in progress. LOCK may be used to prevent external agents from accessing memory which is currently involved in an atomic operation. LOCK is asserted in the first clock of an atomic operation and deasserted in the clock cycle following the last bus access for the atomic operation. To allow the most flexibility for memory system enforcement of locked accesses, the processor acknowledges a bus hold request when LOCK is asserted. The processor performs DMA transfers while LOCK is active.
HOLD	**I** S(L) H(Z) R(Z)	**HOLD REQUEST** signals that an external agent requests access to the external bus. The processor asserts HOLDA after completing the current bus request. HOLD, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents.
BOFF	**I** S(L) H(Z) R(Z)	**BUS BACKOFF**, when asserted, suspends the current access and causes the bus pins to float. When BOFF is deasserted, the ADS signal is asserted on the next clock cycle and the access is resumed.

Table 3. 80960CF Pin Description — External Bus Signals (Sheet 3 of 3)

Name	Type	Description
HOLDA	**O** S H(1) R(Q)	**HOLD ACKNOWLEDGE** indicates to a bus requestor that the processor has relinquished control of the external bus. When HOLDA is asserted, the external address bus, data bus and bus control signals are floated. HOLD, $\overline{\text{BOFF}}$, HOLDA and BREQ are used together to arbitrate access to the processor's external bus by external bus agents. Since the processor grants HOLD requests and enters the Hold Acknowledge state even while $\overline{\text{RESET}}$ is asserted, the state of the HOLDA pin is independent of the $\overline{\text{RESET}}$ pin.
BREQ	**O** S H(Q) R(0)	**BUS REQUEST** is asserted when the bus controller has a request pending. BREQ can be used by external bus arbitration logic in conjunction with HOLD and HOLDA to determine when to return mastership of the external bus to the processor.
D/$\overline{\text{C}}$	**O** S H(Z) R(Z)	**DATA OR CODE** is asserted for a data request and deasserted for instruction requests. D/$\overline{\text{C}}$ has the same timing as W/$\overline{\text{R}}$.
$\overline{\text{DMA}}$	**O** S H(Z) R(Z)	**DMA ACCESS** indicates whether the bus request was initiated by the DMA controller. $\overline{\text{DMA}}$ is asserted for any DMA request. $\overline{\text{DMA}}$ is deasserted for all other requests.
$\overline{\text{SUP}}$	**O** S H(Z) R(Z)	**SUPERVISOR ACCESS** indicates whether the bus request is issued while in supervisor mode. $\overline{\text{SUP}}$ is asserted when the request has supervisor privileges and is deasserted otherwise. $\overline{\text{SUP}}$ can be used to isolate supervisor code and data structures from non-supervisor requests.

Table 4. 80960CF Pin Description — Processor Control Signals (Sheet 1 of 2)

Name	Type	Description
$\overline{\text{RESET}}$	**I** A(L) H(Z) R(Z)	**RESET** causes the chip to reset. When $\overline{\text{RESET}}$ is asserted, all external signals return to the reset state. When $\overline{\text{RESET}}$ is deasserted, initialization begins. When the 2-x clock mode is selected, $\overline{\text{RESET}}$ must remain asserted for 32 CLKIN cycles before being deasserted to guarantee correct processor initialization. When the 1-x clock mode is selected, $\overline{\text{RESET}}$ must remain asserted for 10,000 CLKIN cycles before being deasserted to guarantee correct processor initialization. The CLKMODE pin selects 1-x or 2-x input clock division of the CLKIN pin. The Hold Acknowledge bus state functions while the chip is reset. If the bus is in the Hold Acknowledge state when $\overline{\text{RESET}}$ is asserted, the processor internally resets, but maintains the Hold Acknowledge state on external pins until the Hold request is removed. If a Hold request is made while the processor is in the reset state, the processor bus grants HOLDA and enters the Hold Acknowledge state.
$\overline{\text{FAIL}}$	**O** S H(Q) R(0)	**FAIL** indicates failure of the self-test performed at initialization. When $\overline{\text{RESET}}$ is deasserted and initialization begins, the $\overline{\text{FAIL}}$ pin is asserted. An internal self-test is performed as part of the initialization process. If this self-test passes, the $\overline{\text{FAIL}}$ pin is deasserted; otherwise it remains asserted. The $\overline{\text{FAIL}}$ pin is reasserted while the processor performs an external bus self-confidence test. If this self-test passes, the processor deasserts the $\overline{\text{FAIL}}$ pin and branches to the user's initialization routine; otherwise the $\overline{\text{FAIL}}$ pin remains asserted. Internal self-test and the use of the $\overline{\text{FAIL}}$ pin can be disabled with the STEST pin.
STEST	**I** S(L) H(Z) R(Z)	**SELF TEST** enables or disables the internal self-test feature at initialization. STEST is read on the rising edge of $\overline{\text{RESET}}$. When asserted, internal self-test and external bus confidence tests are performed during processor initialization. When deasserted, only the bus confidence tests are performed during initialization.
$\overline{\text{ONCE}}$	**I** A(L) H(Z) R(Z)	**ON CIRCUIT EMULATION**, when asserted, causes all outputs to be floated. $\overline{\text{ONCE}}$ is continuously sampled while $\overline{\text{RESET}}$ is low and is latched on the rising edge of $\overline{\text{RESET}}$. To place the processor in the ONCE state: (1) assert $\overline{\text{RESET}}$ and $\overline{\text{ONCE}}$ (order does not matter) (2) wait for at least 16 CLKIN periods in 2-x mode—or 10,000 CLKIN periods in 1-x mode—after V_{CC} and CLKIN are within operating specifications (3) deassert $\overline{\text{RESET}}$ (4) wait at least 32 CLKIN periods (The processor will now be latched in the ONCE state while $\overline{\text{RESET}}$ is high.) To exit the ONCE state, bring V_{CC} and CLKIN to operating conditions, then assert $\overline{\text{RESET}}$ and bring $\overline{\text{ONCE}}$ high prior to deasserting $\overline{\text{RESET}}$. CLKIN must operate within the specified operating conditions until Step 4 completes. CLKIN may then be changed to DC to achieve the lowest possible ONCE mode leakage current. $\overline{\text{ONCE}}$ can be used by emulator products or board testers to effectively make an installed processor transparent in the board.

Table 4. 80960CF Pin Description — Processor Control Signals (Sheet 2 of 2)

Name	Type	Description
CLKIN	**I** A(E) H(Z) R(Z)	**CLOCK INPUT** is an input for the external clock needed to run the processor. The external clock is internally divided as prescribed by the CLKMODE pin to produce PCLK2:1.
CLKMODE	**I** A(L) H(Z) R(Z)	**CLOCK MODE** selects the division factor applied to the external clock input (CLKIN). When CLKMODE is high, CLKIN is divided by one to create PCLK2:1 and the processor's internal clock. When CLKMODE is low, CLKIN is divided by two to create PCLK2:1 and the processor's internal clock. CLKMODE should be tied high or low in a system as the clock mode is not latched by the processor. If left unconnected, the processor internally pulls the CLKMODE pin low, enabling the 2-x clock mode.
PCLK2:1	**O** S H(Q) R(Q)	**PROCESSOR OUTPUT CLOCKS** provide a timing reference for all inputs and outputs. All input and output timings are specified in relation to PCLK2 and PCLK1. PCLK2 and PCLK1 are identical signals. Two output pins are provided to allow flexibility in the system's allocation of capacitive loading on the clock. PCLK2:1 may also be connected at the processor to form a single clock signal.
V_{SS}	–	**GROUND** connections must be connected externally to a V_{SS} board plane.
V_{CC}	–	**POWER** connections must be connected externally to a V_{CC} board plane.
V_{CCPLL}	–	**V_{CCPLL}** is a separate V_{CC} supply pin for the phase lock loop used in 1-x clock mode. Connecting a simple lowpass filter to V_{CCPLL} may help reduce clock jitter (T_{CP}) in noisy environments. Otherwise, V_{CCPLL} should be connected to V_{CC}.
NC	–	**NO CONNECT** pins must not be connected in a system.

Table 5. 80960CF Pin Description — DMA and Interrupt Unit Control Signals

Name	Type	Description
DREQ3:0	**I** A(L) H(Z) R(Z)	**DMA REQUEST** is used to request a DMA transfer. Each of the four signals requests a transfer on a single channel. DREQ0 requests channel 0, DREQ1 requests channel 1, etc. When two or more channels are requested simultaneously, the channel with the highest priority is serviced first. Channel priority mode is programmable.
DACK3:0	**O** S H(1) R(1)	**DMA ACKNOWLEDGE** indicates that a DMA transfer is being executed. Each of the four signals acknowledges a transfer for a single channel. DACK0 acknowledges channel 0, DACK1 acknowledges channel 1, etc. DACK3:0 are asserted when the requesting device of a DMA is accessed.
EOP/TC3:0	**I/O** A(L) H(Z/Q) R(Z)	**END OF PROCESS/TERMINAL COUNT** can be programmed as either an input (EOP3:0) or output (TC3:0), but not both. Each pin is individually programmable. When programmed as an input, EOPx causes termination of a current DMA transfer for the channel that corresponds to the EOPx pin. EOP0 corresponds to channel 0, EOP1 corresponds to channel 1, etc. When a channel is configured for source *and* destination chaining, the EOP pin for that channel causes termination of only the current buffer transferred and causes the next buffer to be transferred. EOP3:0 are asynchronous inputs. When programmed as an output, the channel's TCx pin indicates that the channel byte count has reached 0 and a DMA has terminated. TCx is driven with the same timing as DACKx during the last DMA transfer for a buffer. If the last bus request is executed as multiple bus accesses, TCx stays asserted for the entire bus request.
XINT7:0	**I** A(E/L) H(Z) R(Z)	**EXTERNAL INTERRUPT PINS** cause interrupts to be requested. These pins can be configured in three modes: **Dedicated Mode:** each pin is a dedicated external interrupt source. Dedicated inputs can be individually programmed to be level (low) or edge (falling) activated. **Expanded Mode:** the eight pins act together as an 8-bit vectored interrupt source. The interrupt pins in this mode are level activated. Since the interrupt pins are active low, the vector number requested is the 1's complement of the positive logic value place on the port. This eliminates glue logic to interface to combinational priority encoders which output negative logic. **Mixed Mode:** XINT7:5 are dedicated sources and XINT4:0 act as the five most significant bits of an expanded mode vector. The least significant bits are set to 010 internally.
NMI	**I** A(E) H(Z) R(Z)	**NON-MASKABLE INTERRUPT** causes a non-maskable interrupt event to occur. NMI is the highest priority interrupt recognized. NMI is an edge (falling) activated source.

3.3 80960CF Mechanical Data

3.3.1 80960CF PGA PINOUT

Figure 2 depicts the complete 80960CF PGA pinout as viewed from the top side of the component (i.e., pins facing down). Figure 3 shows the complete 80960CF PGA pinout as viewed from the pin-side of the package (i.e., pins facing up).

Table 6 lists the 80960CF pin names and package location in signal order; Table 7 lists the pin names and package location in pin order. See **Section 4.0, ELECTRICAL SPECIFICATIONS** for specifications and recommended connections.

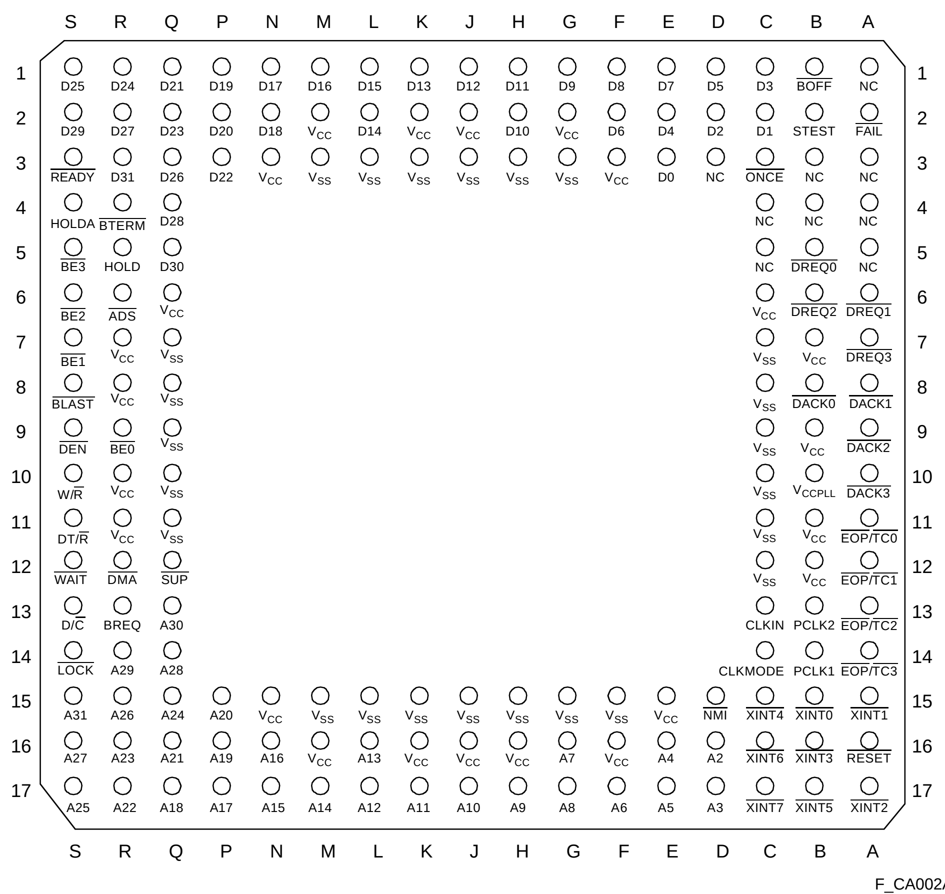


Figure 2. 80960CF PGA Pinout — View from Top (Pins Facing Down)

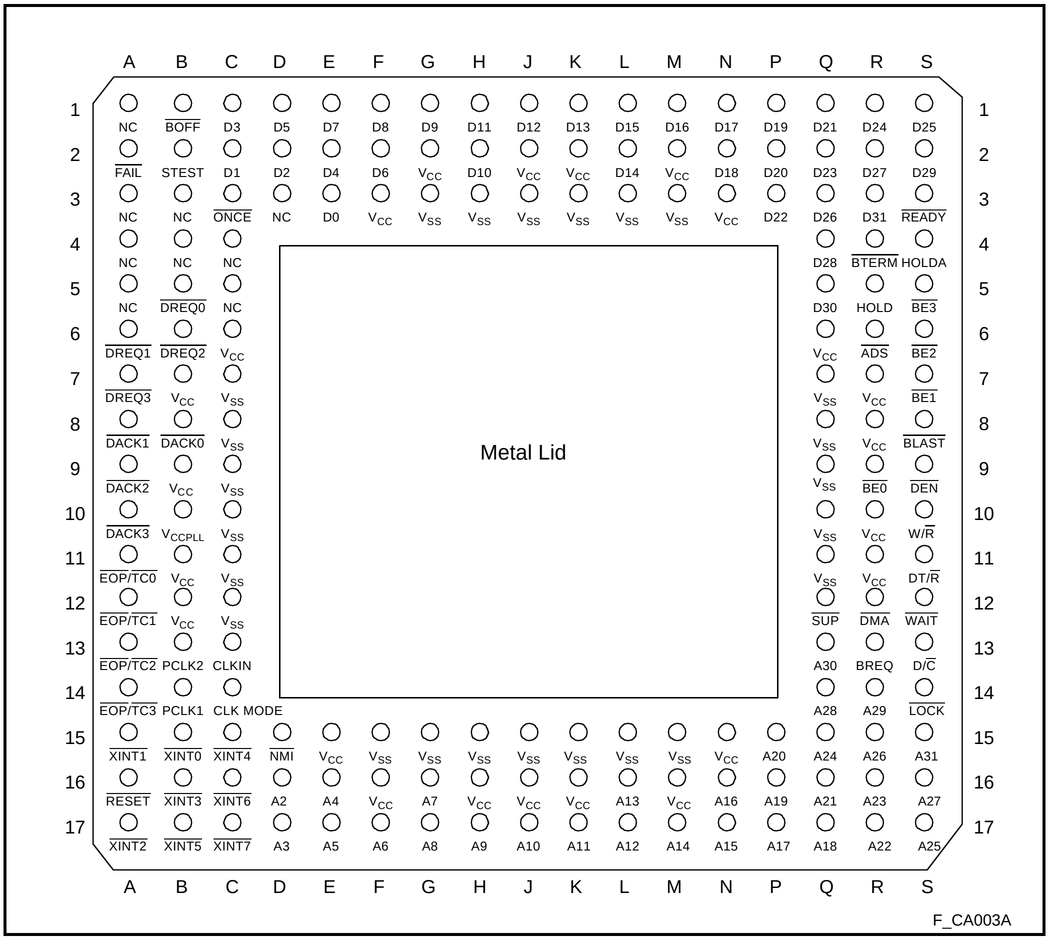


Figure 3. 80960CF PGA Pinout — View from Bottom (Pins Facing Up)

Table 6. 80960CF PGA Pinout — In Signal Order

Address Bus		Data Bus		Bus Control		Processor Control		I/O	
Signal	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**	**Signal**	**Pin**
A31	S15	D31	R3	$\overline{\text{BE3}}$	S5	$\overline{\text{RESET}}$	A16	$\overline{\text{DREQ3}}$	A7
A30	Q13	D30	Q5	$\overline{\text{BE2}}$	S6			$\overline{\text{DREQ2}}$	B6
A29	R14	D29	S2	$\overline{\text{BE1}}$	S7	$\overline{\text{FAIL}}$	A2	$\overline{\text{DREQ1}}$	A6
A28	Q14	D28	Q4	$\overline{\text{BE0}}$	R9			$\overline{\text{DREQ0}}$	B5
A27	S16	D27	R2			STEST	B2		
A26	R15	D26	Q3	W/$\overline{\text{R}}$	S10			$\overline{\text{DACK3}}$	A10
A25	S17	D25	S1			$\overline{\text{ONCE}}$	C3	$\overline{\text{DACK2}}$	A9
A24	Q15	D24	R1	$\overline{\text{ADS}}$	R6			$\overline{\text{DACK1}}$	A8
A23	R16	D23	Q2			CLKIN	C13	$\overline{\text{DACK0}}$	B8
A22	R17	D22	P3	$\overline{\text{READY}}$	S3	CLKMODE	C14		
A21	Q16	D21	Q1	$\overline{\text{BTERM}}$	R4	PLCK1	B14	$\overline{\text{EOP}}$/$\overline{\text{TC3}}$	A14
A20	P15	D20	P2			PLCK2	B13	$\overline{\text{EOP}}$/$\overline{\text{TC2}}$	A13
A19	P16	D19	P1	$\overline{\text{WAIT}}$	S12			$\overline{\text{EOP}}$/$\overline{\text{TC1}}$	A12
A18	Q17	D18	N2	$\overline{\text{BLAST}}$	S8	**V_{SS}**		$\overline{\text{EOP}}$/$\overline{\text{TC0}}$	A11
A17	P17	D17	N1			*Location*			
A16	N16	D16	M1	DT/$\overline{\text{R}}$	S11	C7, C8, C9, C10, C11, C12, F15, G3, G15, H3, H15, J3, J15, K3, K15, L3, L15, M3, M15, Q7, Q8, Q9, Q10, Q11		$\overline{\text{XINT7}}$	C17
A15	N17	D15	L1	$\overline{\text{DEN}}$	S9			$\overline{\text{XINT6}}$	C16
A14	M17	D14	L2					$\overline{\text{XINT5}}$	B17
A13	L16	D13	K1	$\overline{\text{LOCK}}$	S14			$\overline{\text{XINT4}}$	C15
A12	L17	D12	J1					$\overline{\text{XINT3}}$	B16
A11	K17	D11	H1			**V_{CC}**		$\overline{\text{XINT2}}$	A17
A10	J17	D10	H2	HOLD	R5	*Location*		$\overline{\text{XINT1}}$	A15
A9	H17	D9	G1	HOLDA	S4	B7, B9, B11, B12, C6, E15, F3, F16, G2, H16, J2, J16, K2, K16, M2, M16, N3, N15, Q6, R7, R8, R10, R11		$\overline{\text{XINT0}}$	B15
A8	G17	D8	F1	BREQ	R13				
A7	G16	D7	E1					$\overline{\text{NMI}}$	D15
A6	F17	D6	F2	D/$\overline{\text{C}}$	S13				
A5	E17	D5	D1	$\overline{\text{DMA}}$	R12				
A4	E16	D4	E2	$\overline{\text{SUP}}$	Q12	V_{CCPLL}	B10		
A3	D17	D3	C1			**No Connect**			
A2	D16	D2	D2	$\overline{\text{BOFF}}$	B1	*Location*			
		D1	C2			A1, A3, A4, A5, B3, B4, C4, C5, D3			
		D0	E3						

Table 7. 80960CF PGA Pinout — In Pin Order

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	NC	C1	D3	G1	D9	M1	D16	R1	D24
A2	$\overline{\text{FAIL}}$	C2	D1	G2	V_{CC}	M2	V_{CC}	R2	D27
A3	NC	C3	$\overline{\text{ONCE}}$	G3	V_{SS}	M3	V_{SS}	R3	D31
A4	NC	C4	NC	G15	V_{SS}	M15	V_{SS}	R4	$\overline{\text{BTERM}}$
A5	NC	C5	NC	G16	A7	M16	V_{CC}	R5	HOLD
A6	$\overline{\text{DREQ1}}$	C6	V_{CC}	G17	A8	M17	A14	R6	$\overline{\text{ADS}}$
A7	$\overline{\text{DREQ3}}$	C7	V_{SS}					R7	V_{CC}
A8	$\overline{\text{DACK1}}$	C8	V_{SS}	H1	D11	N1	D17	R8	V_{CC}
A9	$\overline{\text{DACK2}}$	C9	V_{SS}	H2	D10	N2	D18	R9	$\overline{\text{BE0}}$
A10	$\overline{\text{DACK3}}$	C10	V_{SS}	H3	V_{SS}	N3	V_{CC}	R10	V_{CC}
A11	$\overline{\text{EOP}}/\overline{\text{TC0}}$	C11	V_{SS}	H15	V_{SS}	N15	V_{CC}	R11	V_{CC}
A12	$\overline{\text{EOP}}/\overline{\text{TC1}}$	C12	V_{SS}	H16	V_{CC}	N16	A16	R12	$\overline{\text{DMA}}$
A13	$\overline{\text{EOP}}/\overline{\text{TC2}}$	C13	CLKIN	H17	A9	N17	A15	R13	BREQ
A14	$\overline{\text{EOP}}/\overline{\text{TC3}}$	C14	CLKMODE					R14	A29
A15	$\overline{\text{XINT1}}$	C15	$\overline{\text{XINT4}}$	J1	D12	P1	D19	R15	A26
A16	$\overline{\text{RESET}}$	C16	$\overline{\text{XINT6}}$	J2	V_{CC}	P2	D20	R16	A23
A17	$\overline{\text{XINT2}}$	C17	$\overline{\text{XINT7}}$	J3	V_{SS}	P3	D22	R17	A22
				J15	V_{SS}	P15	A20		
B1	$\overline{\text{BOFF}}$	D1	D5	J16	V_{CC}	P16	A19	S1	D25
B2	STEST	D2	D2	J17	A10	P17	A17	S2	D29
B3	NC	D3	NC					S3	$\overline{\text{READY}}$
B4	NC	D15	$\overline{\text{NMI}}$	K1	D13	Q1	D21	S4	HOLDA
B5	$\overline{\text{DREQ0}}$	D16	A2	K2	V_{CC}	Q2	D23	S5	$\overline{\text{BE3}}$
B6	$\overline{\text{DREQ2}}$	D17	A3	K3	V_{SS}	Q3	D26	S6	$\overline{\text{BE2}}$
B7	V_{CC}			K15	V_{SS}	Q4	D28	S7	$\overline{\text{BE1}}$
B8	$\overline{\text{DACK0}}$	E1	D7	K16	V_{CC}	Q5	D30	S8	$\overline{\text{BLAST}}$
B9	V_{CC}	E2	D4	K17	A11	Q6	V_{CC}	S9	$\overline{\text{DEN}}$
B10	V_{CCPLL}	E3	D0			Q7	V_{SS}	S10	$\text{W}/\overline{\text{R}}$
B11	V_{CC}	E15	V_{CC}	L1	D15	Q8	V_{SS}	S11	$\text{DT}/\overline{\text{R}}$
B12	V_{CC}	E16	A4	L2	D14	Q9	V_{SS}	S12	$\overline{\text{WAIT}}$
B13	PCLK2	E17	A5	L3	V_{SS}	Q10	V_{SS}	S13	$\text{D}/\overline{\text{C}}$
B14	PCLK1			L15	V_{SS}	Q11	V_{SS}	S14	$\overline{\text{LOCK}}$
B15	$\overline{\text{XINT0}}$	F1	D8	L16	A13	Q12	$\overline{\text{SUP}}$	S15	A31
B16	$\overline{\text{XINT3}}$	F2	D6	L17	A12	Q13	A30	S16	A27
B17	$\overline{\text{XINT5}}$	F3	V_{CC}			Q14	A28	S17	A25
		F15	V_{SS}			Q15	A24		
		F16	V_{CC}			Q16	A21		
		F17	A6			Q17	A18		

3.4 Package Thermal Specifications

The 80960CF is specified for operation when T_C (case temperature) is within the range of 0°C–85°C. T_C may be measured in any environment to determine whether the 80960CF is within specified operating range. Case temperature should be measured at the center of the top surface, opposite the pins. Refer to Figure 4.

T_A (ambient temperature) is calculated from θ_{CA} (thermal resistance from case to ambient) using the equation:

$$T_A = T_C - P^*\theta_{CA}$$

Table 8 shows the maximum T_A allowable (without exceeding T_C) at various airflows and operating frequencies (f_{PCLK}).

Note that T_A is greatly improved by attaching fins or a heatsink to the package. P (maximum power consumption) is calculated by using the typical I_{CC} as tabulated in **Section 4.4, DC Specifications** and V_{CC} of 5V.

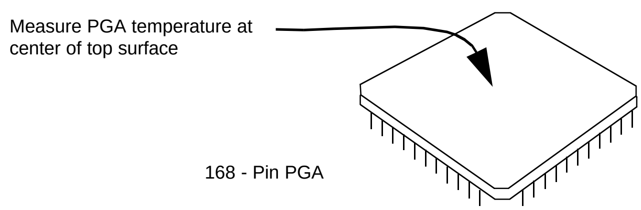


Figure 4. Measuring 80960CF PGA Case Temperature

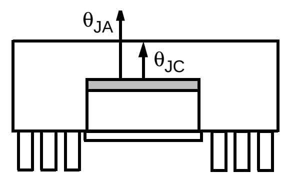
Table 8. Maximum T_A at Various Airflows in °C (PGA Package Only)

	f_{PCLK} (MHz)	Airflow-ft/min (m/sec)					
		0 (0)	**200 (1.01)**	**400 (2.03)**	**600 (3.04)**	**800 (4.06)**	**1000 (5.07)**
T_A with Heatsink*	40	20	40	58	60	66	68
T_A without Heatsink*	40	0	15	30	40	50	52

NOTES:
*0.285” high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

Table 9. 80960CF PGA Package Thermal Characteristics

Thermal Resistance — °C/Watt						
Parameter	**Airflow — ft./min (m/sec)**					
	0 (0)	**200 (1.01)**	**400 (2.03)**	**600 (3.07)**	**800 (4.06)**	**1000 (5.07)**
θ Junction-to-Case (Case measured as shown in Figure 4)	1.5	1.5	1.5	1.5	1.5	1.5
θ Case-to-Ambient (No Heatsink)	17	14	11	9	7.1	6.6
θ Case-to-Ambient (With Heatsink)*	13	9	5.5	5	3.9	3.4



NOTES:

1. This table applies to 80960CF PGA plugged into socket or soldered directly to board.
2. $\theta_{JA} = \theta_{JC} + \theta_{CA}$

*0.285" high unidirectional heatsink (Al alloy 6061, 50 mil fin width, 150 mil center-to-center fin spacing).

3.5 Stepping Register Information

Upon reset, register g0 contains die stepping information (Figure 5). The most significant byte contains ASCII 0; the upper middle byte contains an ASCII C; the lower middle byte contains an ASCII F. The least significant byte contains the stepping number in ASCII. g0 retains this information until it is overwritten by the user program. Table 10 contains a cross reference of the number in the least significant byte of register g0 to the die stepping number.

	MSB			LSB
ASCII	00	43	46	Stepping Number
DECIMAL	0	C	F	Stepping Number

Figure 5. Register g0

Table 10. Die Stepping Cross Reference

g0 Least Significant Byte	Die Stepping
01	A
02	B
03	C
04	D
05	E

3.6 Sources for Accessories

The following is a list of suggested sources for 80960CF accessories. This is neither an endorsement or a warranty of the performance of any of the listed products and/or companies.

Sockets

1. 3M Textool Test and Interconnection Products
   P.O. Box 2963
   Austin, TX 78769-2963
2. Augat, Inc. Interconnection Products Group
   33 Perry Avenue, P.O. box 779
   Attleboro, MA 02703
   (508) 699-7646
3. Concept Mfg, Inc. Decoupling Sockets)
   41484 Christy Street
   Fremont, CA 94538
   (415) 651-3804

Heatsinks/Fins

1. Thermalloy, Inc.
   2021 West Valley View Lane
   Dallas, TX 75234-8993
   (214) 243-4321 FAX: (214) 241-4656
2. E G & G Division
   60 Audubon Road
   Wakefield, MA 01880
   (617) 245-5900

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute Maximum Ratings

Parameter	Maximum Rating
Storage Temperature	–65°C to +150°C
Case Temperature Under Bias	–65°C to +110°C
Supply Voltage wrt. V_{SS}	–0.5V to + 6.5V
Voltage on Other Pins wrt. V_{SS}	–0.5V to V_{CC} + 0.5V

NOTICE: This data sheet contains information on products in the sampling and initial production phases of development. It is valid for the devices indicated in the revision history. The specifications are subject to change without notice.

***WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

4.2 Operating Conditions

Table 11. Operating Conditions (80960CF-40)

Symbol	Parameter		Min	Max	Units	Notes
V_{CC}	Supply Voltage	80960CF-40	4.75	5.25	V	
f_{CLK2x}	Input Clock Frequency (2-x Mode)	80960CF-40	0	80	MHz	
f_{CLK1x}	Input Clock Frequency (1-x Mode)	80960CF-40	8	40	MHz	(1)
T_C	Case Temp Under Bias, PGA Pkg.	80960CF-40	0	85	°C	

NOTES:

1. When in the 1-x input clock mode, CLKIN is an input to an internal phase-locked loop and must maintain a minimum frequency of 8 MHz for proper processor operation. However, in the 1-x mode, CLKIN may still be stopped when the processor is in a reset condition. If CLKIN is stopped, the specified $\overline{\text{RESET}}$ low time must be provided once CLKIN restarts and has stabilized.

4.3 Recommended Connections

Power and ground connections must be made to multiple V_{CC} and V_{SS} (GND) pins. Every 80960CF-based circuit board should include power (V_{CC}) and ground (V_{SS}) planes for power distribution. Every V_{CC} pin must be connected to the power plane, and every V_{SS} pin must be connected to the ground plane. Pins identified as "NC" **must not** be connected in the system.

Liberal decoupling capacitance should be placed near the 80960CF. The processor can cause transient power surges when its numerous output buffers transition, particularly when connected to large capacitive loads.

Low inductance capacitors and interconnects are recommended for best high frequency electrical performance. Inductance can be reduced by shortening the board traces between the processor and decoupling capacitors as much as possible. Capacitors specifically designed for PGA packages will offer the lowest possible inductance.

For reliable operation, always connect unused inputs to an appropriate signal level. In particular, any unused interrupt ($\overline{\text{XINT}}$, $\overline{\text{NMI}}$) or DMA ($\overline{\text{DREQ}}$) input should be connected to V_{CC} through a pull-up resistor, as should $\overline{\text{BTERM}}$ if not used. Pull-up resistors should be in the in the range of 20 KΩ for each pin tied high. If $\overline{\text{READY}}$ or HOLD are not used, the unused input should be connected to ground. **N.C. pins must always remain unconnected.** For additional information refer to the *i960® Cx Microprocessor User's Guide* (#270710).

4.4 DC Specifications

Table 12. DC Characteristics

(80960CF-40 under the conditions described in **Section 4.2, Operating Conditions**.)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage for all pins except $\overline{RESET}$	– 0.3	+0.8	V	
V_{IH}	Input High Voltage for all pins except $\overline{RESET}$	2.0	V_{CC} + 0.3	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 5 mA
V_{OH}	Output High Voltage I_{OH} = –1 mA I_{OH} = – 200 µA	2.4 V_{CC} – 0.5		V V	
V_{ILR}	Input Low Voltage for $\overline{RESET}$	– 0.3	1.5	V	
V_{IHR}	Input High Voltage for $\overline{RESET}$	3.5	V_{CC} + 0.3	V	
I_{LI1}	Input Leakage Current for each pin *except*: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, STEST, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{NMI}$, $\overline{XINT7:0}$, $\overline{BOFF}$, $\overline{READY}$, HOLD, CLKMODE		±15	µA	$0 \le V_{IN} \le V_{CC}$ (1)
I_{LI2}	Input Leakage Current for: $\overline{BTERM}$, $\overline{ONCE}$, $\overline{DREQ3:0}$, STEST, $\overline{EOP3:0}$/$\overline{TC3:0}$, $\overline{NMI}$, $\overline{XINT7:0}$, $\overline{BOFF}$	0	– 300	µA	V_{IN} = 0.45V (2)
I_{LI3}	Input Leakage Current for: $\overline{READY}$, HOLD, CLKMODE	0	500	µA	V_{IN} = 2.4V (3,7)
I_{LO}	Output Leakage Current		±15	µA	$0.45 \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current (80960CF-40): I_{CC} Max I_{CC} Typ		 1150 1000	 mA mA	 (4) (5)
I_{ONCE}	ONCE-mode Supply Current		200	mA	
C_{IN}	Input Capacitance for: CLKIN, $\overline{RESET}$, $\overline{ONCE}$, $\overline{READY}$, HOLD, $\overline{DREQ3:0}$, $\overline{BOFF}$, $\overline{XINT7:0}$, $\overline{NMI}$, $\overline{BTERM}$, CLKMODE	0	12	pF	F_C = 1 MHz
C_{OUT}	Output Capacitance of each output pin		12	pF	F_C = 1 MHz (6)
$C_{I/O}$	I/O Pin Capacitance		12	pF	F_C = 1 MHz

NOTES:

1. No pullup or pulldown.
2. These pins have internal pullup resistors.
3. These pins have internal pulldown resistors.
4. Measured at worst case frequency, V_{CC} and temperature, with device operating and outputs loaded to the test conditions described in **Section 4.5.1, AC TEST CONDITIONS.**
5. I_{CC} Typical is not tested.
6. Output Capacitance is the capacitive load of a floating output.
7. CLKMODE pin has a pulldown resistor only when $\overline{ONCE}$ pin is deasserted.

4.5 AC Specifications

Table 13. 80960CF AC Characteristics (40 MHz) (Sheet 1 of 2)

(80960CF-40 only, per the conditions in **4.2 Operating Conditions** and **4.5.1 AC TEST CONDITIONS**.)

Symbol	Parameter		Min	Max	Units	Notes
Input Clock (1,9)						
T_F	CLKIN Frequency		0	80	MHz	
T_C	CLKIN Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	25 12.5	125 ∞	ns ns	(11)
T_{CS}	CLKIN Period Stability	In 1-x Mode (f_{CLK1x})		±0.1%	Δ	(12)
T_{CH}	CLKIN High Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(11)
T_{CL}	CLKIN Low Time	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	5 5	62.5 ∞	ns ns	(11)
T_{CR}	CLKIN Rise Time		0	6	ns	
T_{CF}	CLKIN Fall Time		0	6	ns	
Output Clocks (1,8)						
T_{CP}	CLKIN to PCLK2:1 Delay	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	– 2 2	2 25	ns ns	(3,12) (3)
T	PCLK2:1 Period	In 1-x Mode (f_{CLK1x}) In 2-x Mode (f_{CLK2x})	T_C $2T_C$		ns ns	(12) (3)
T_{PH}	PCLK2:1 High Time		(T/2) – 2	T/2	ns	(12)
T_{PL}	PCLK2:1 Low Time		(T/2) – 2	T/2	ns	(12)
T_{PR}	PCLK2:1 Rise Time		1	4	ns	(3)
T_{PF}	PCLK2:1 Fall Time		1	4	ns	(3)
Synchronous Outputs (8)						
T_{OH} T_{OV}	Output Valid Delay, Output Hold					(6,10)
	T_{OH1}, T_{OV1}	A31:2	3	14	ns	
	T_{OH2}, T_{OV2}	$\overline{BE3:0}$	3	16	ns	
	T_{OH3}, T_{OV3}	$\overline{ADS}$	6	16	ns	
	T_{OH4}, T_{OV4}	W/$\overline{R}$	3	16	ns	
	T_{OH5}, T_{OV5}	D/$\overline{C}$, $\overline{SUP}$, $\overline{DMA}$	4	16	ns	
	T_{OH6}, T_{OV6}	$\overline{BLAST}$, $\overline{WAIT}$	5	16	ns	
	T_{OH7}, T_{OV7}	$\overline{DEN}$	3	16	ns	
	T_{OH8}, T_{OV8}	HOLDA, $\overline{BREQ}$	4	16	ns	
	T_{OH9}, T_{OV9}	$\overline{LOCK}$	4	16	ns	
	T_{OH10}, T_{OV10}	$\overline{DACK3:0}$	4	16	ns	
	T_{OH11}, T_{OV11}	D31:0	3	16	ns	
	T_{OH12}, T_{OV12}	DT/$\overline{R}$	T/2 + 3	T/2 + 14	ns	
	T_{OH13}, T_{OV13}	$\overline{FAIL}$	2	14	ns	
	T_{OH14}, T_{OV14}	$\overline{EOP3:0}$/$\overline{TC3:0}$	3	16	ns	(6,10)
T_{OF}	Output Float for all outputs		3	22	ns	(6)

NOTES:
See Table 14 (following this table) for all notes related to AC specifications.

Table 13. 80960CF AC Characteristics (40 MHz) (Sheet 2 of 2)
(80960CF-40 only, per the conditions in **4.2 Operating Conditions** and **4.5.1 AC TEST CONDITIONS**.)

Symbol	Parameter	Min	Max	Units	Notes
Synchronous Inputs (1,9,10)					
T_{IS}	Input Setup T_{IS1} D31:0 T_{IS2} $\overline{BOFF}$ T_{IS3} $\overline{BTERM}/READY$ T_{IS4} HOLD	 3 15 7 5		 ns ns ns ns	
T_{IH}	Input Hold T_{IH1} D31:0 T_{IH2} $\overline{BOFF}$ T_{IH3} $\overline{BTERM}/READY$ T_{IH4} HOLD	 5 5 2 3		 ns ns ns ns	
Relative Output Timings (1,2,3,8)					
T_{AVSH1}	A31:2 Valid to $\overline{ADS}$ Rising	T – 4	T + 4	ns	
T_{AVSH2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, D/$\overline{C}$, $\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{ADS}$ Rising	T – 6	T + 6	ns	
T_{AVEL1}	A31:2 Valid to $\overline{DEN}$ Falling	T – 4	T + 4	ns	
T_{AVEL2}	$\overline{BE3:0}$, W/$\overline{R}$, $\overline{SUP}$, $\overline{INST}$,$\overline{DMA}$, $\overline{DACK3:0}$ Valid to $\overline{DEN}$ Falling	T – 6	T + 6	ns	
T_{NLQV}	$\overline{WAIT}$ Falling to Output Data Valid	± 6		ns	
T_{DVNH}	Output Data Valid to $\overline{WAIT}$ Rising	N*T – 6	N*T + 6	ns	(4)
T_{NLNH}	$\overline{WAIT}$ Falling to $\overline{WAIT}$ Rising	N*T ± 4		ns	(4)
T_{NHQX}	Output Data Hold after $\overline{WAIT}$ Rising	(N+1)*T–8	(N+1)*T+6	ns	(5)
T_{EHTV}	DT/$\overline{R}$ Hold after $\overline{DEN}$ High	T/2 – 7	∞	ns	(6)
T_{TVEL}	DT/$\overline{R}$ Valid to $\overline{DEN}$ Falling	T/2 – 4		ns	
Relative Input Timings (1,2,3)					
T_{IS5}	$\overline{RESET}$ Input Setup (2-x Clock Mode)	6		ns	(13)
T_{IH5}	$\overline{RESET}$ Input Hold (2-x Clock Mode)	5		ns	(13)
T_{IS6}	$\overline{DREQ3:0}$ Input Setup	12		ns	(7)
T_{IH6}	$\overline{DREQ3:0}$ Input Hold	7		ns	(7)
T_{IS7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Setup	7		ns	(15)
T_{IH7}	$\overline{XINT7:0}$, $\overline{NMI}$ Input Hold	3		ns	(15)
T_{IS8}	$\overline{RESET}$ Input Setup (1-x Clock Mode)	3		ns	(14)
T_{IH8}	$\overline{RESET}$ Input Hold (1-x Clock Mode)	T/4 + 1		ns	(14)

NOTES:
See Table 14 (following this table) for all notes related to AC specifications.

Table 14. AC Characteristics Notes

NOTES:

1. See **Section 4.5.2, AC TIMING WAVEFORMS** for waveforms and definitions.
2. See Figure 15 for capacitive derating information for output delays and hold times.
3. See Figure 16 for capacitive derating information for rise and fall times.
4. Where N is the number of N_{RAD}, N_{RDD}, N_{WAD} or N_{WDD} wait states that are programmed in the Bus Controller Region Table. $\overline{WAIT}$ never goes active when there are no wait states in an access.
5. N = Number of wait states inserted with $\overline{READY}$.
6. Output Data and/or DT/$\overline{R}$ may be driven indefinitely following a cycle if there is no subsequent bus activity.
7. Since asynchronous inputs are synchronized internally by the 80960CF, they have no required setup or hold times to be recognized and for proper operation. However, to guarantee recognition of the input at a particular edge of PCLK2:1, the setup times shown must be met. Asynchronous inputs must be active for at least two consecutive PCLK2:1 rising edges to be seen by the processor.
8. These specifications are guaranteed by the processor.
9. These specifications must be met by the system for proper operation of the processor.
10. This timing is dependent upon the loading of PCLK2:1. Use the derating curves of **Section 4.5.3, DERATING CURVES** to adjust the timing for PCLK2:1 loading.
11. In the 1-x input clock mode, the maximum input clock period is limited to 125 ns while the processor is operating. When the processor is in reset, the input clock may stop even in 1-x mode.
12. When in the 1-x input clock mode, these specifications assume a stable input clock with a period variation of less than ± 0.1% between adjacent cycles.
13. In 2-x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must meet setup and hold times to the falling edge of the CLKIN. (See Figure 21.)
14. In 1-x clock mode, $\overline{RESET}$ is an asynchronous input which has no required setup and hold time for proper operation. However, to guarantee the device exits reset synchronized to a particular clock edge, the $\overline{RESET}$ pin must meet setup and hold times to the rising edge of the CLKIN. (See Figure 22.)
15. The interrupt pins are synchronized internally by the 80960CF. They have no required setup or hold times for proper operation. These pins are sampled by the interrupt controller every other clock and must be active for at least three consecutive PCLK2:1 periods when asserting them asynchronously. To guarantee recognition at a particular clock edge, the setup and hold times shown must be met for two consecutive PCLK2:1 falling edges.

4.5.1 AC TEST CONDITIONS

The AC Specifications in Section 4.5 are tested with the 50 pF load shown in Figure 6. Figure 15 shows how timings vary with load capacitance.

Specifications are measured at the 1.5V crossing point, unless otherwise indicated. Input waveforms are assumed to have a rise and fall time of ≤ 2 ns from 0.8V to 2.0V. See **Section 4.5.2, AC TIMING WAVEFORMS** for AC specification definitions, test points and illustrations.

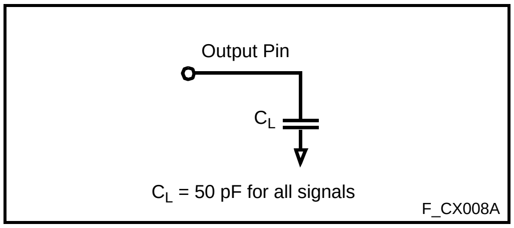


Figure 6. AC Test Load

4.5.2 AC TIMING WAVEFORMS

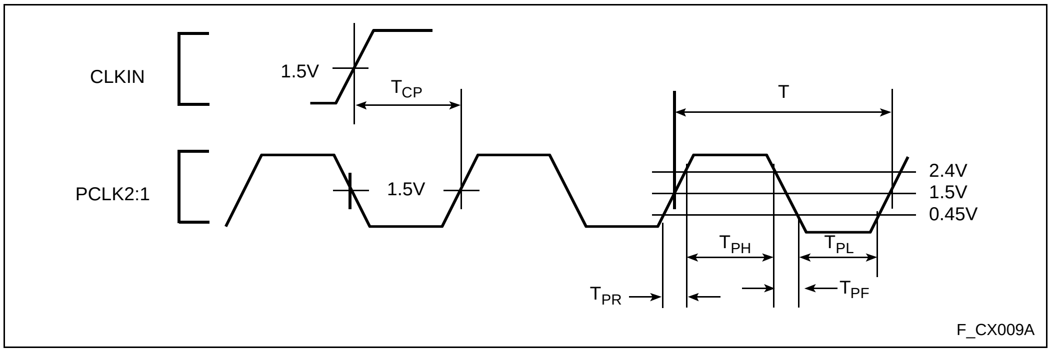


Figure 7. Input and Output Clocks Waveform

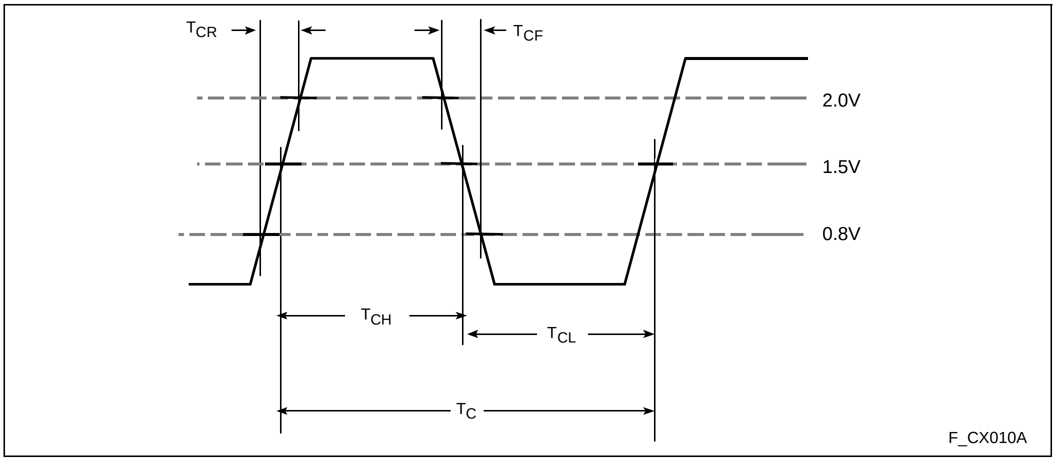
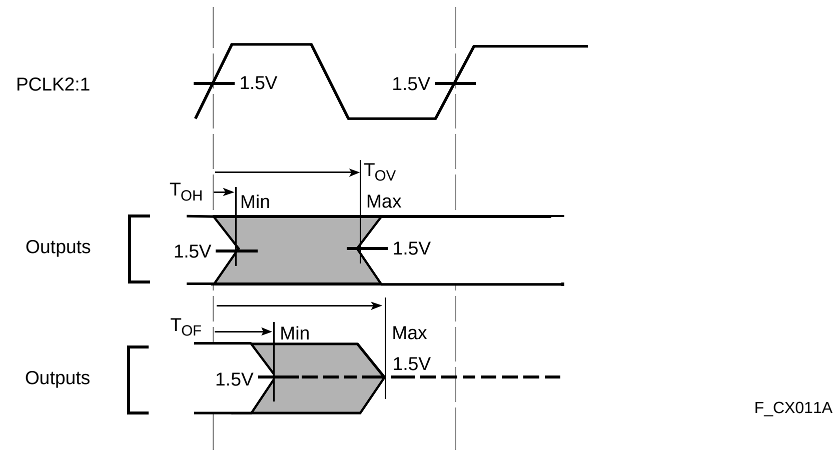


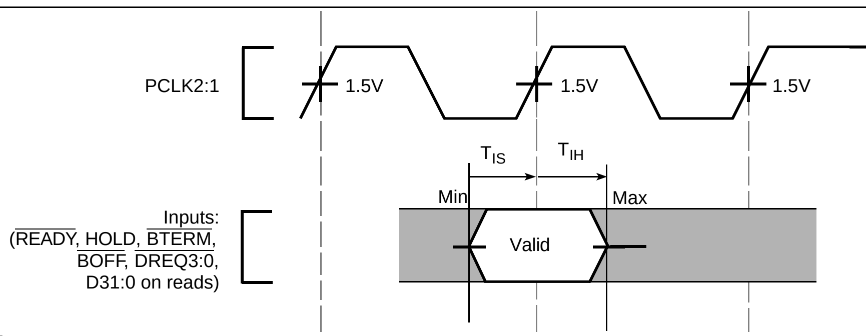
Figure 8. CLKIN Waveform



NOTES:

1. T_{OV} T_{OH} - OUTPUT DELAY - Maximum output delay is referred to as Output Valid Delay (T_{OV}); minimum output delay is referred to as Output Hold (T_{OH}).
2. T_{OF} - OUTPUT FLOAT DELAY - Output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.

Figure 9. Output Delay and Float Waveform



NOTES:

1. T_{IS} T_{IH} - INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

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Figure 10. Input Setup and Hold Waveform

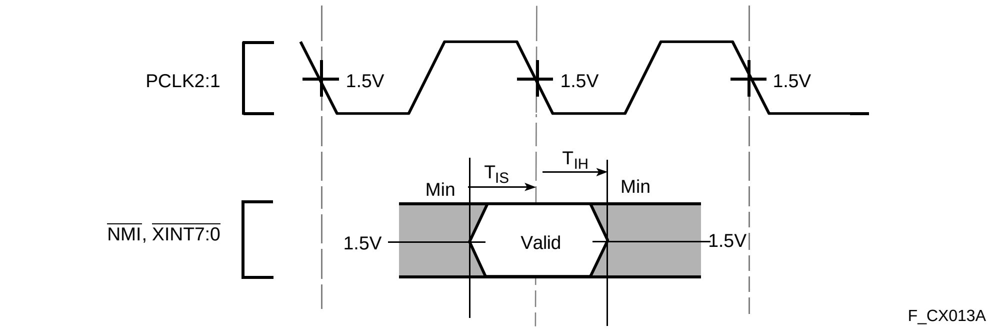
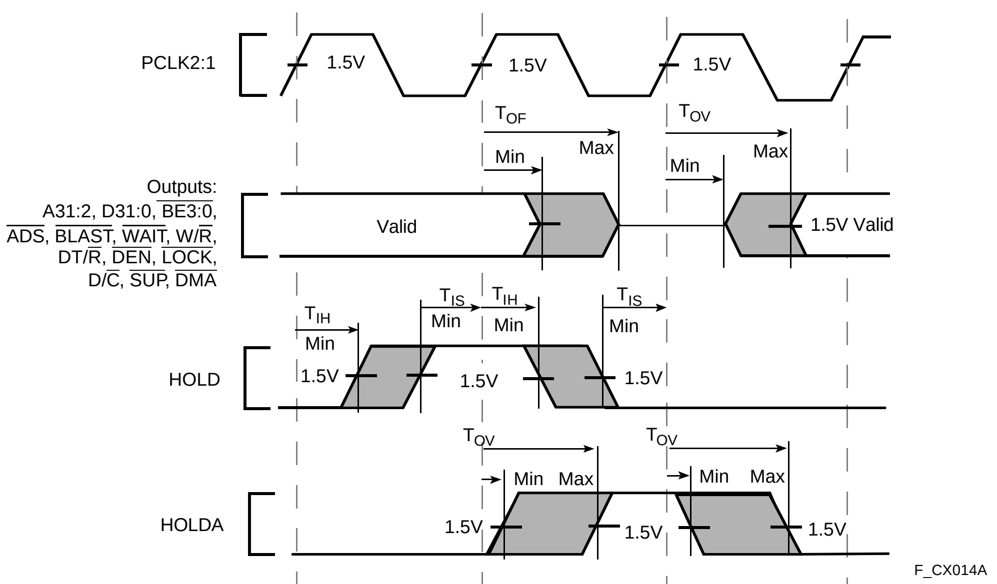


Figure 11. $\overline{NMI}$, $\overline{XINT7:0}$ Input Setup and Hold Waveform



NOTES:

1. T_{OV} T_{OH} - OUTPUT DELAY - Maximum output delay is referred to as Output Valid Delay (T_{OV}); minimum output delay is referred to as Output Hold (T_{OH}).
2. T_{OF} - OUTPUT FLOAT DELAY - Output float condition occurs when the maximum output current becomes less that I_{LO} in magnitude.
3. T_{IS} T_{IH} - INPUT SETUP AND HOLD - The input setup and hold requirements specify the sampling window during which synchronous inputs must be stable for correct processor operation.

Figure 12. Hold Acknowledge Timings

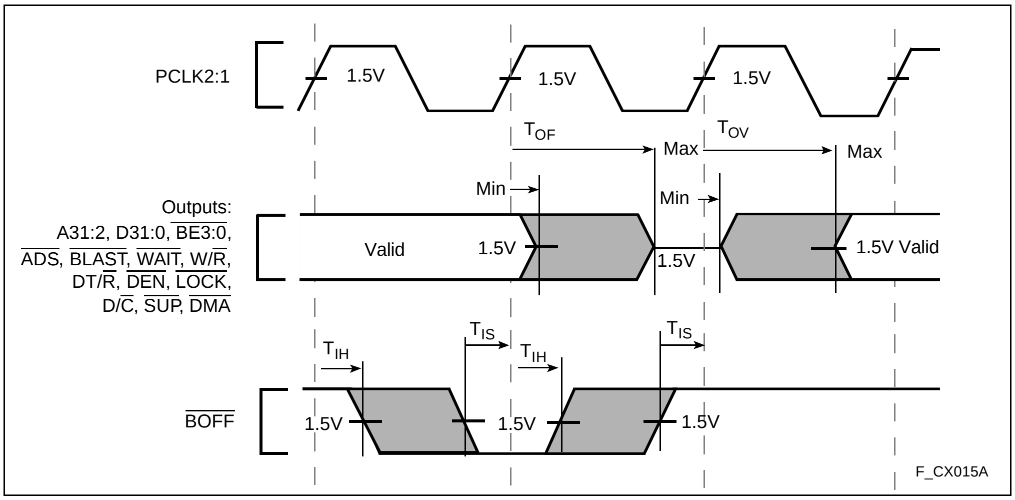


Figure 13. Bus Backoff (BOFF) Timings

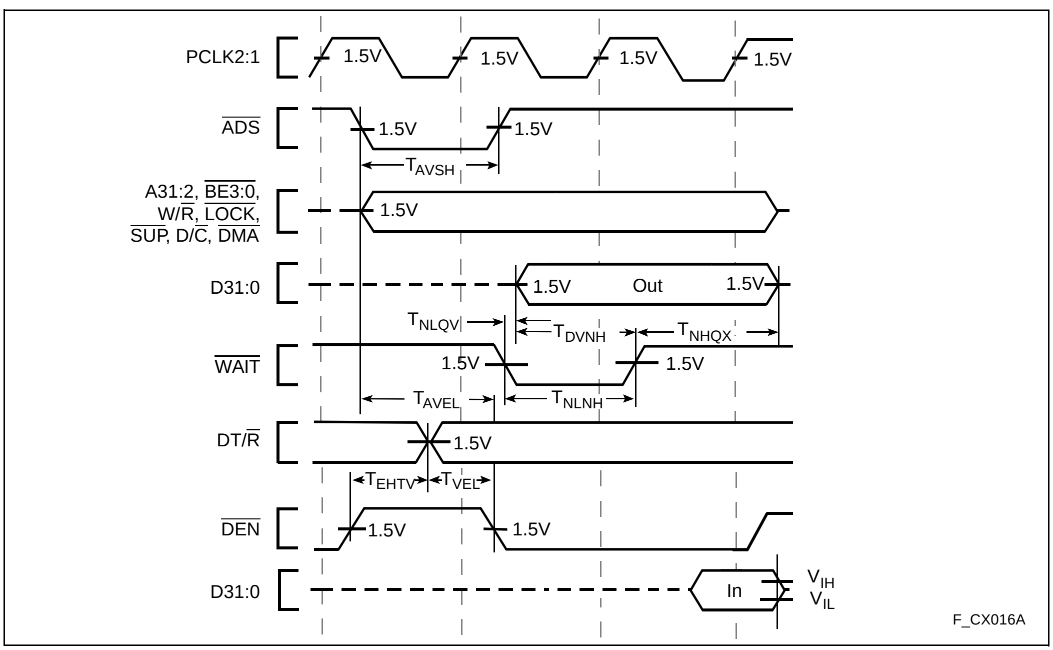


Figure 14. Relative Timings Waveforms

ERRATA ON THIS PAGE

Section	Rev.	Description
Figure 15. Output Delay or Hold vs. Load Capacitance	-001	In the legend, the dashed line and the solid line were reversed.
Figure 17. ICC vs. Frequency and Temperature	-001	Tc tags were incorrectly reversed; T_C = 85° C should be TOP line

4.5.3 DERATING CURVES

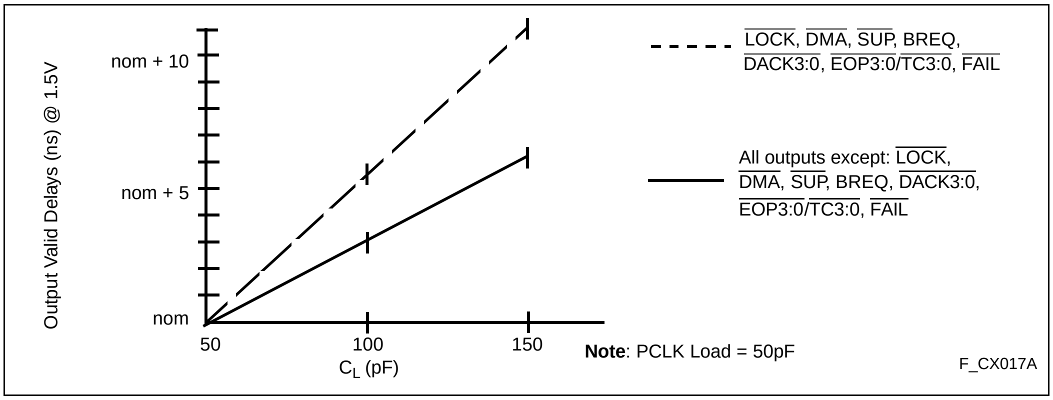


Figure 15. Output Delay or Hold vs. Load Capacitance

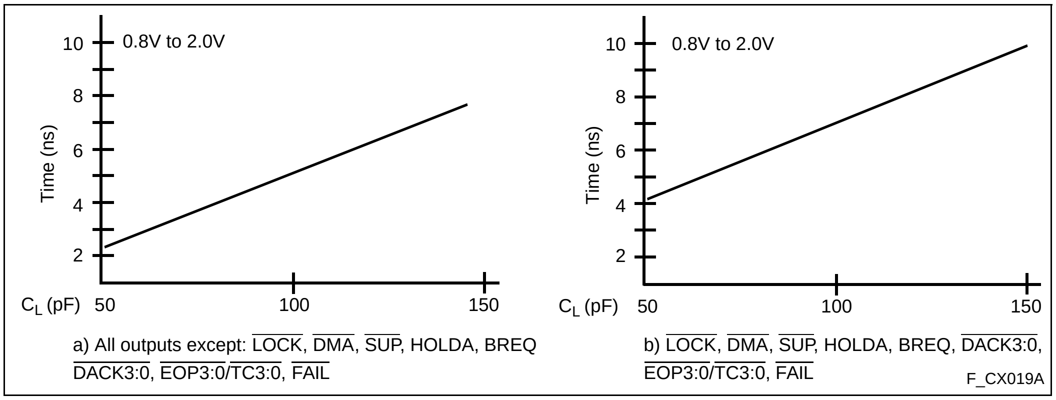


Figure 16. Rise and Fall Time Derating at Highest Operating Temperature and Minimum V_{CC}

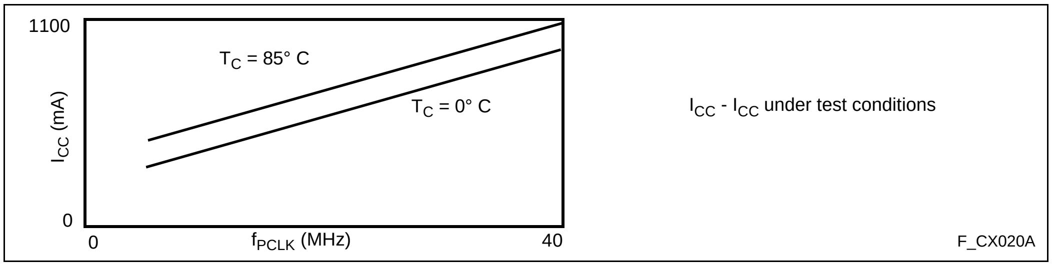


Figure 17. I_{CC} vs. Frequency and Temperature

5.0 RESET, BACKOFF AND HOLD ACKNOWLEDGE

Table 15 lists the condition of each processor output pin while $\overline{\text{RESET}}$ is asserted (low). Table 16 lists the condition of each processor output pin while HOLDA is asserted (high).

In Table 15, with regard to bus output pin state only, the Hold Acknowledge state takes precedence over the reset state. Although asserting the $\overline{\text{RESET}}$ pin internally resets the processor, the processor's bus output pins do not enter the reset state if Hold Acknowledge has been granted to a previous HOLD request (HOLDA is active). Furthermore, the processor grants new HOLD requests and enters the Hold Acknowledge state even while in reset.

For example, if HOLD is asserted while HOLDA is inactive and the processor is in the reset state, the processor's bus pins enter the Hold Acknowledge state and HOLDA is granted. The processor is not able to perform memory accesses until the HOLD request is removed, even if the $\overline{\text{RESET}}$ pin is brought high. This operation is provided to simplify boot-up synchronization among multiple processors sharing the same bus.

Table 15. Reset Conditions (Sheet 1 of 2)

Pins	State During Reset (HOLDA inactive)
A31:2	Floating
D31:0	Floating
$\overline{\text{BE3:0}}$	Driven high (Inactive)
W/$\overline{\text{R}}$	Driven low (Read)
$\overline{\text{ADS}}$	Driven high (Inactive)
$\overline{\text{WAIT}}$	Driven high (Inactive)
$\overline{\text{BLAST}}$	Driven low (Active)
DT/$\overline{\text{R}}$	Driven low (Receive)
$\overline{\text{DEN}}$	Driven high (Inactive)
$\overline{\text{LOCK}}$	Driven high (Inactive)
BREQ	Driven low (Inactive)
D/$\overline{\text{C}}$	Floating
$\overline{\text{DMA}}$	Floating

Table 15. Reset Conditions (Sheet 2 of 2)

Pins	State During Reset (HOLDA inactive)
$\overline{\text{SUP}}$	Floating
$\overline{\text{FAIL}}$	Driven low (Active)
$\overline{\text{DACK3:0}}$	Driven high (Inactive)
$\overline{\text{EOP3:0/TC3:0}}$	Floating (Set to input mode)

Table 16. Hold Acknowledge and Backoff Conditions

Pins	State During HOLDA
A31:2	Floating
D31:0	Floating
$\overline{\text{BE3:0}}$	Floating
W/$\overline{\text{R}}$	Floating
$\overline{\text{ADS}}$	Floating
$\overline{\text{WAIT}}$	Floating
$\overline{\text{BLAST}}$	Floating
DT/$\overline{\text{R}}$	Floating
$\overline{\text{DEN}}$	Floating
$\overline{\text{LOCK}}$	Floating
BREQ	Driven (High or low)
D/$\overline{\text{C}}$	Floating
$\overline{\text{DMA}}$	Floating
$\overline{\text{SUP}}$	Floating
$\overline{\text{FAIL}}$	Driven high (Inactive)
$\overline{\text{DACK3:0}}$	Driven high (Inactive)
$\overline{\text{EOP3:0/TC3:0}}$	Driven (If output)

6.0 BUS WAVEFORMS

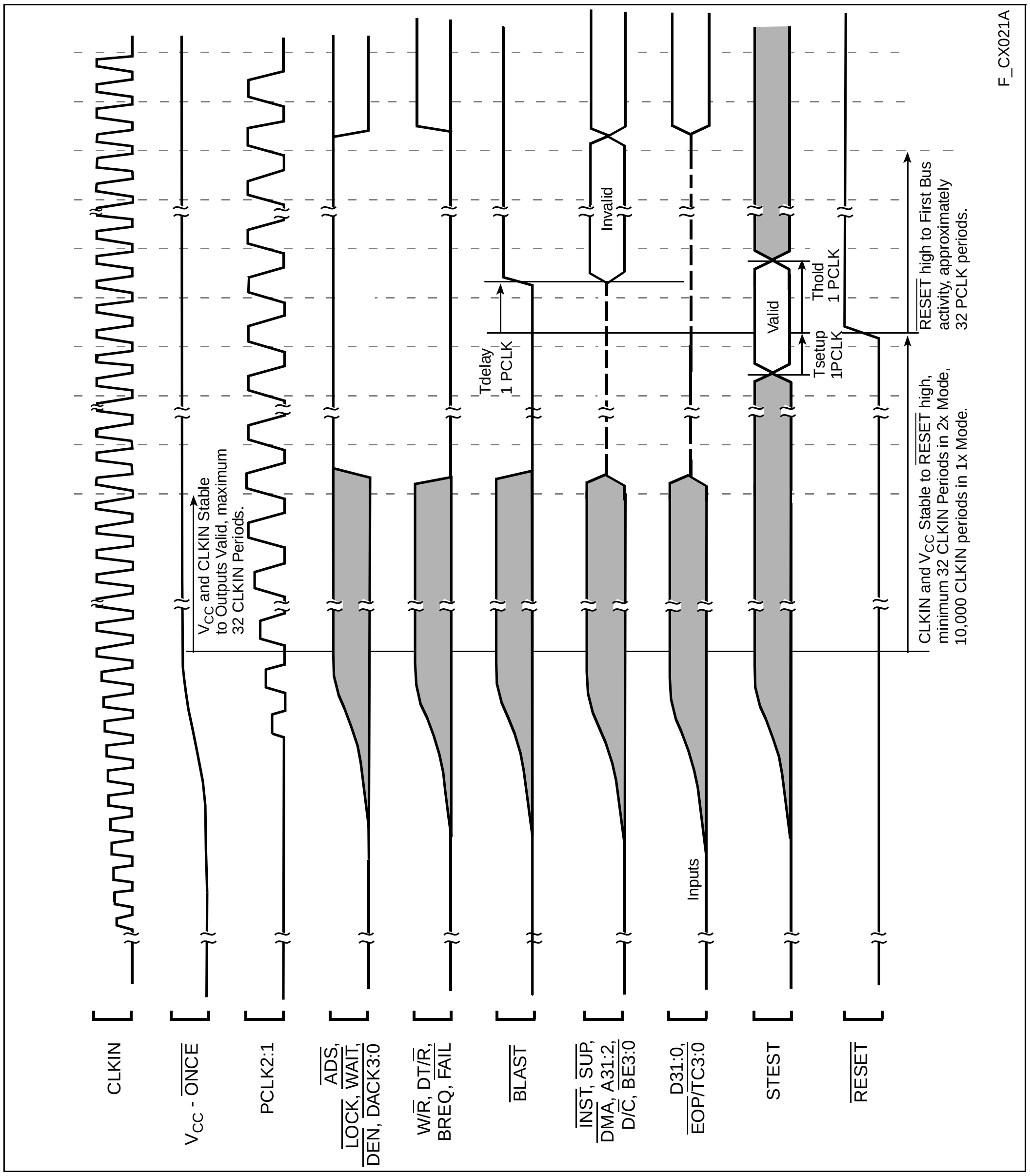


Figure 18. Cold Reset Waveform

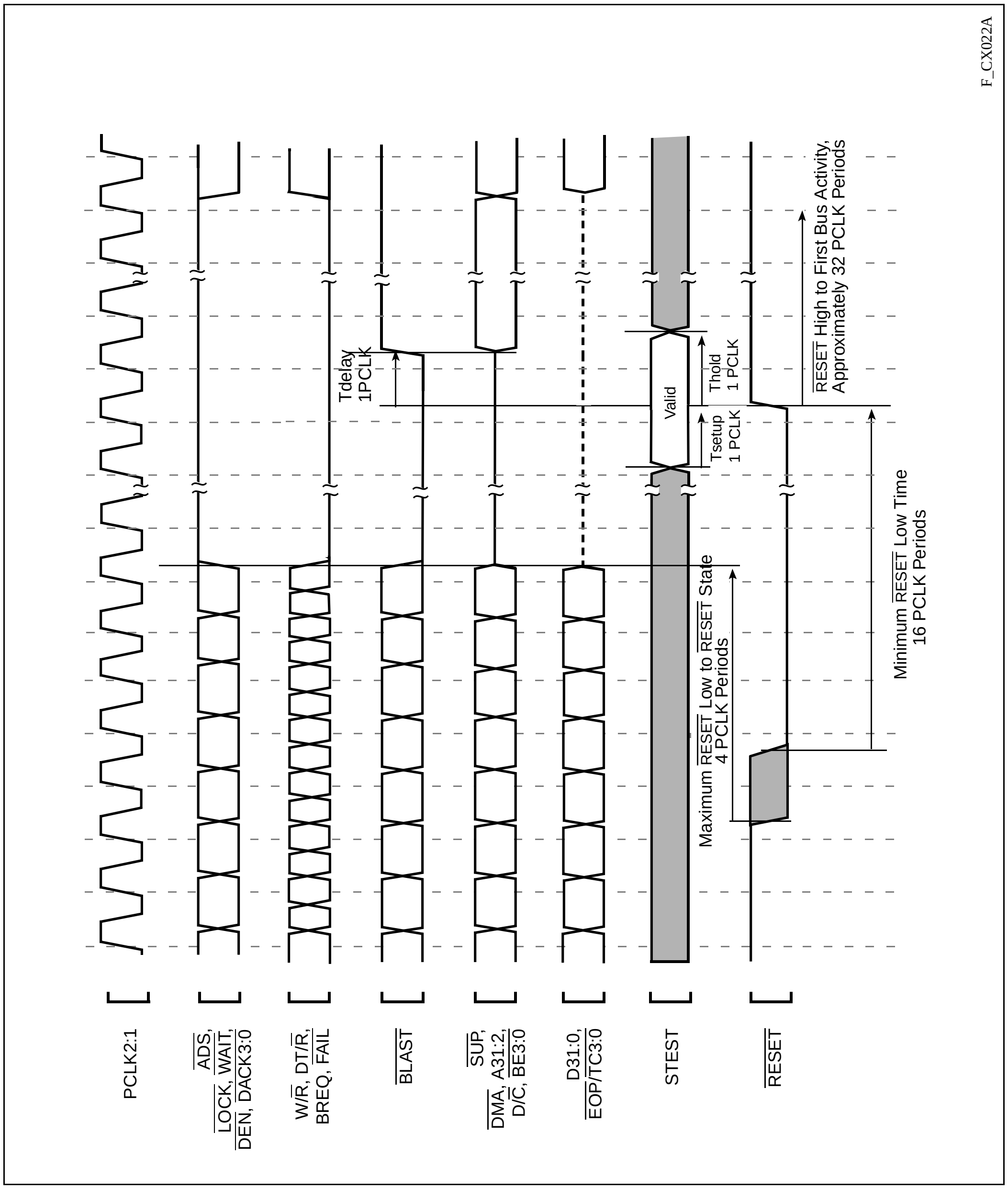


Figure 19. Warm Reset Waveform

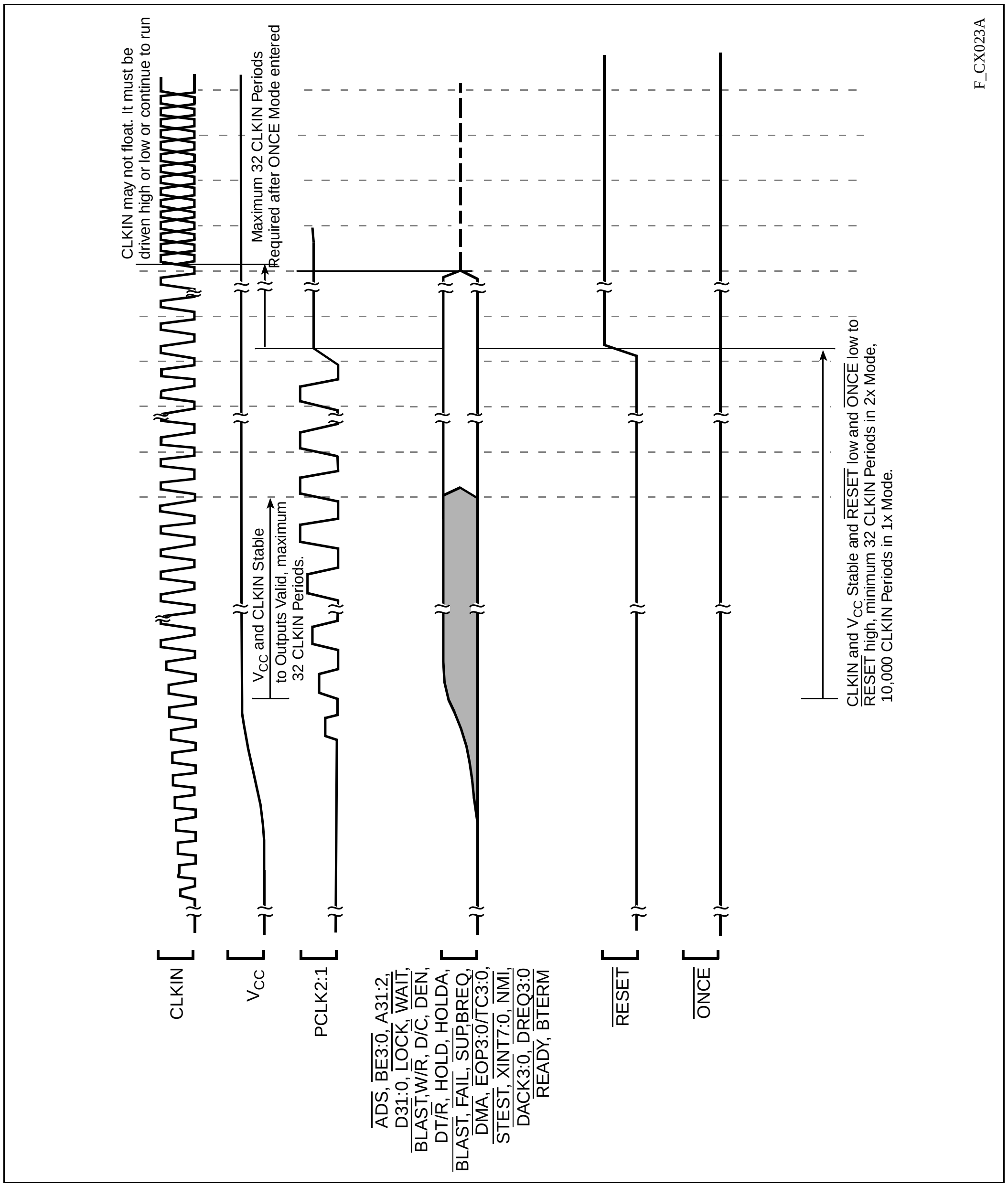
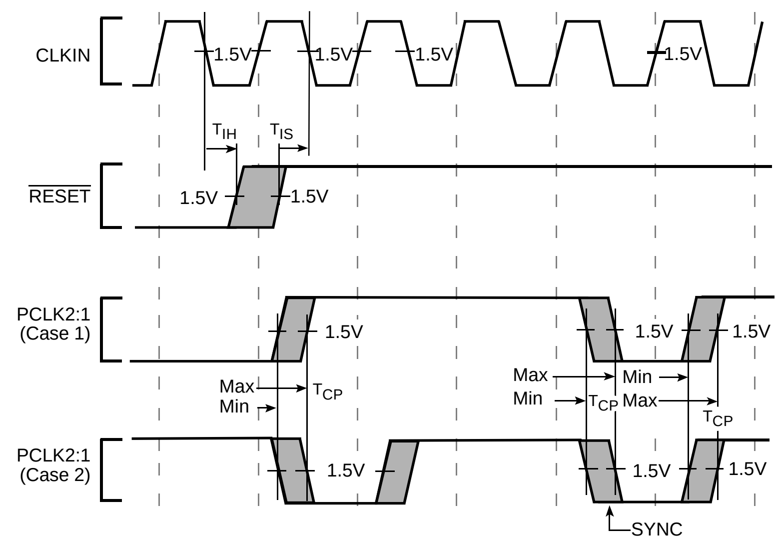


Figure 20. Entering the ONCE State



Note: Case 1 and Case 2 show two possible polarities of PCLK2:1

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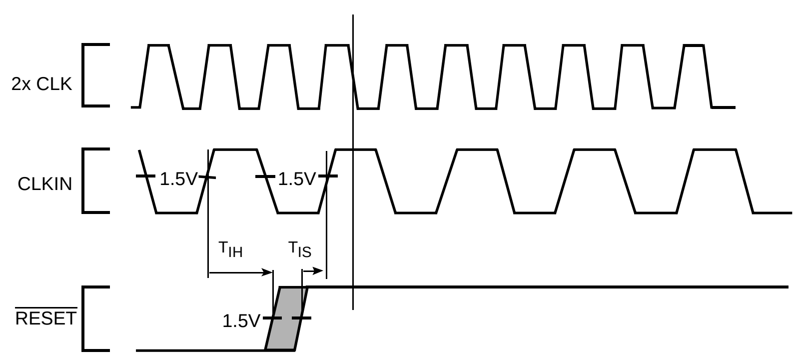
Figure 21. Clock Synchronization in the 2-x Clock Mode



Note: In 1x clock mode, the $\overline{\text{RESET}}$ pin is actually sampled on the falling edge of 2xCLK. 2xCLK is an internal signal generated by the PLL and is not available on an external pin. Therefore, $\overline{\text{RESET}}$ is specified relative to the rising edge of CLKIN. The $\overline{\text{RESET}}$ pin is sampled when PCLK is high.

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Figure 22. Clock Synchronization in the 1-x Clock Mode

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	X xx	X xx	0 00000	0 00	X xx	0 00000	OFF 0	Disabled 0	Disabled 0

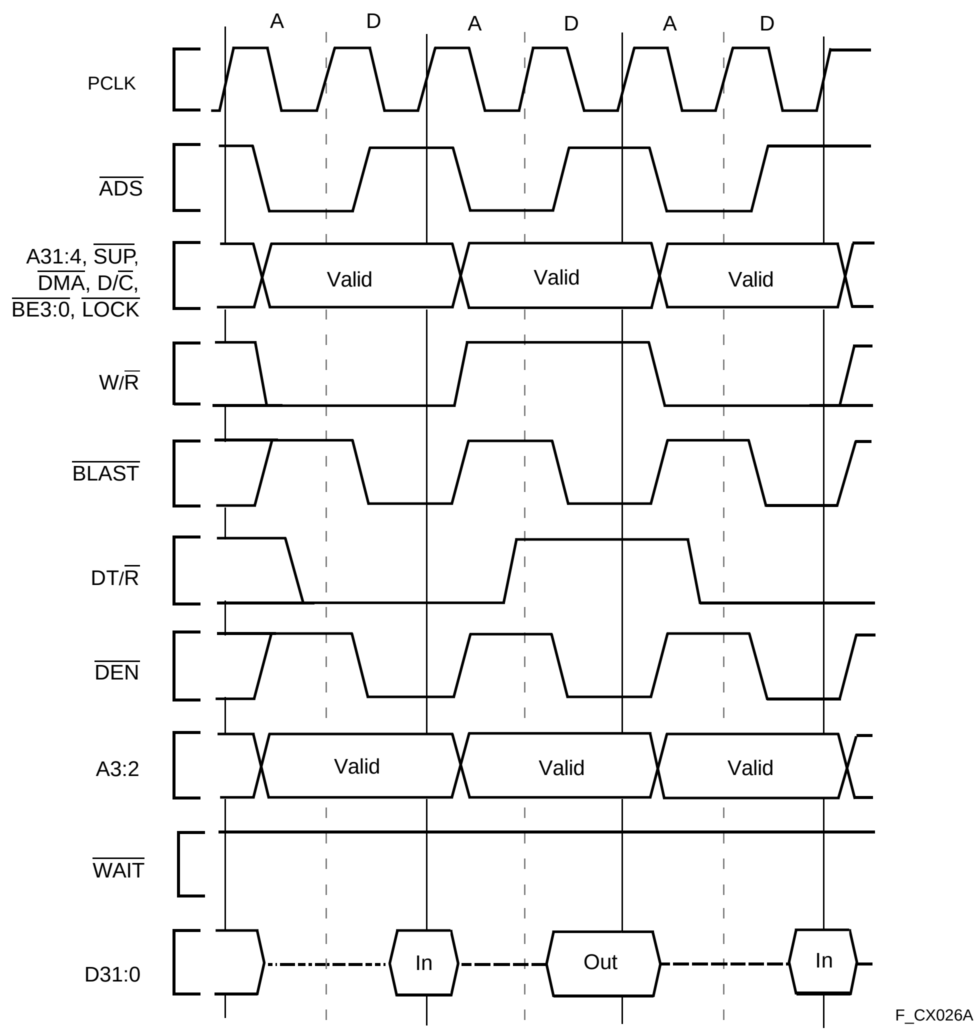


Figure 23. Non-Burst, Non-Pipelined Requests Without Wait States

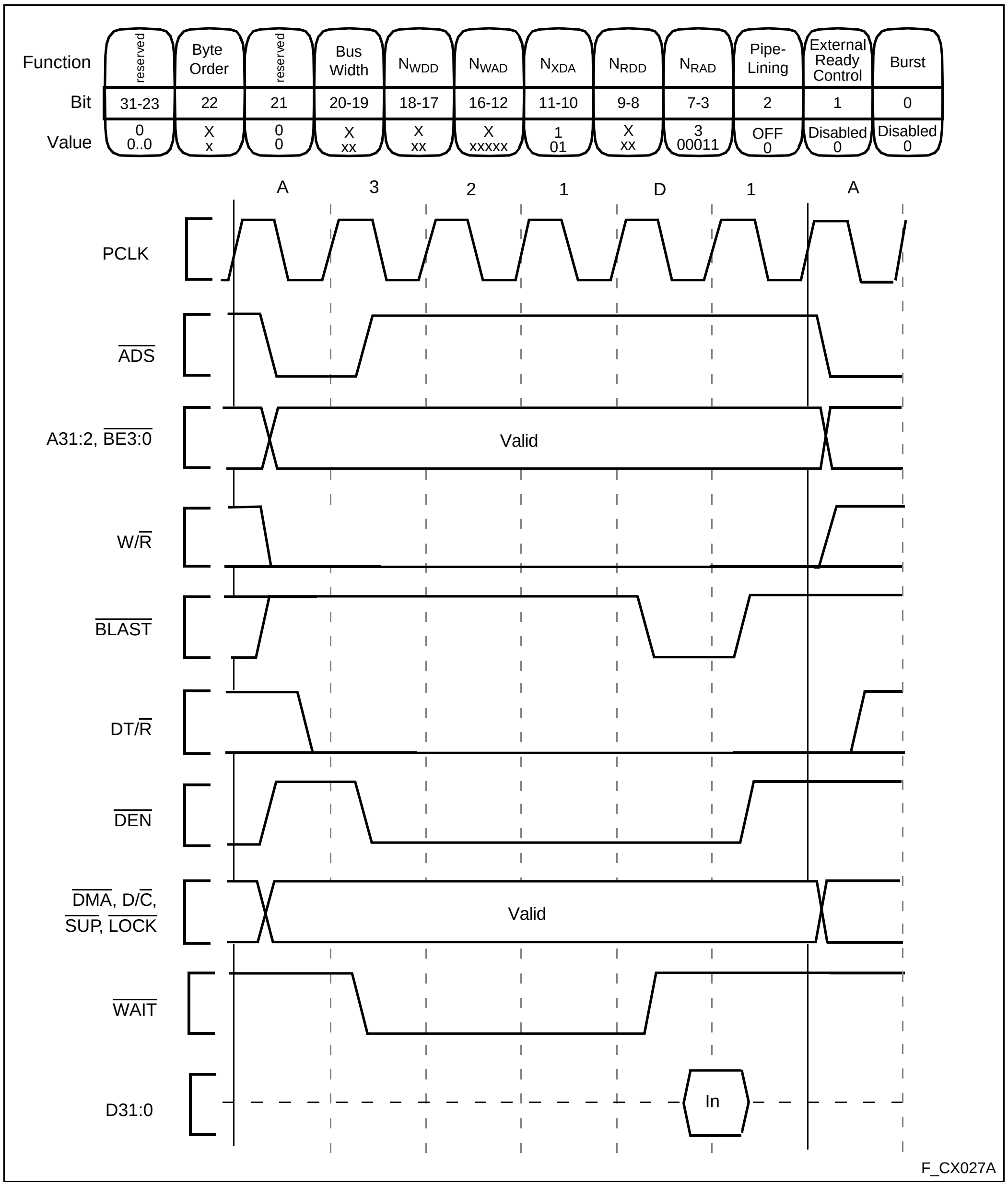


Figure 24. Non-Burst, Non-Pipelined Read Request With Wait States

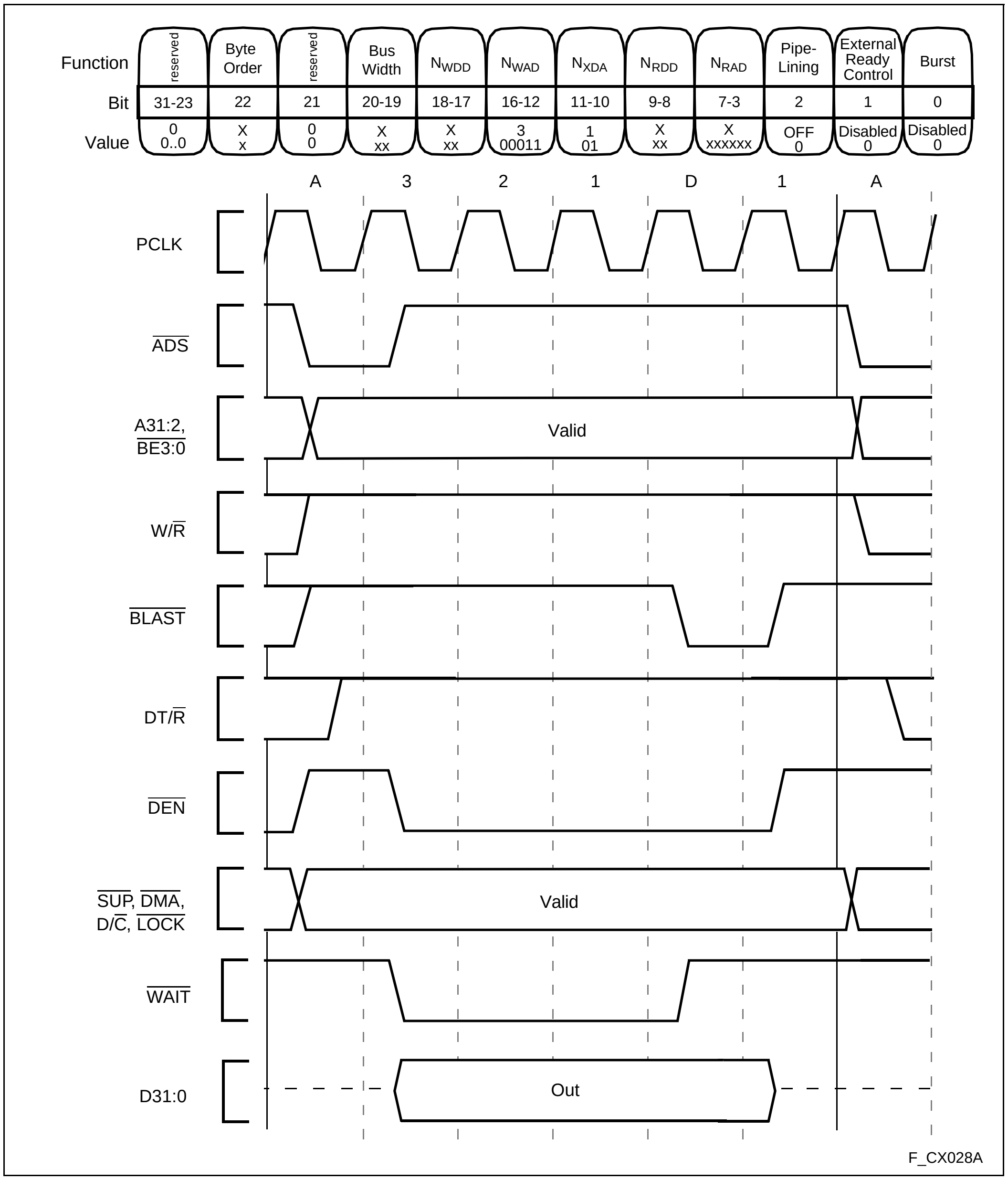


Figure 25. Non-Burst, Non-Pipelined Write Request With Wait States

Function	reserved	Byte Order	reserved	Bus Width	N_{WDD}	N_{WAD}	N_{XDA}	N_{RDD}	N_{RAD}	Pipe-Lining	External Ready Control	Burst
Bit	31-23	22	21	20-19	18-17	16-12	11-10	9-8	7-3	2	1	0
Value	0 0..0	X x	0 0	32-Bit 10	X xx	X xxxxx	0 00	0 00	0 00000	OFF 0	Disabled 0	Enabled 1

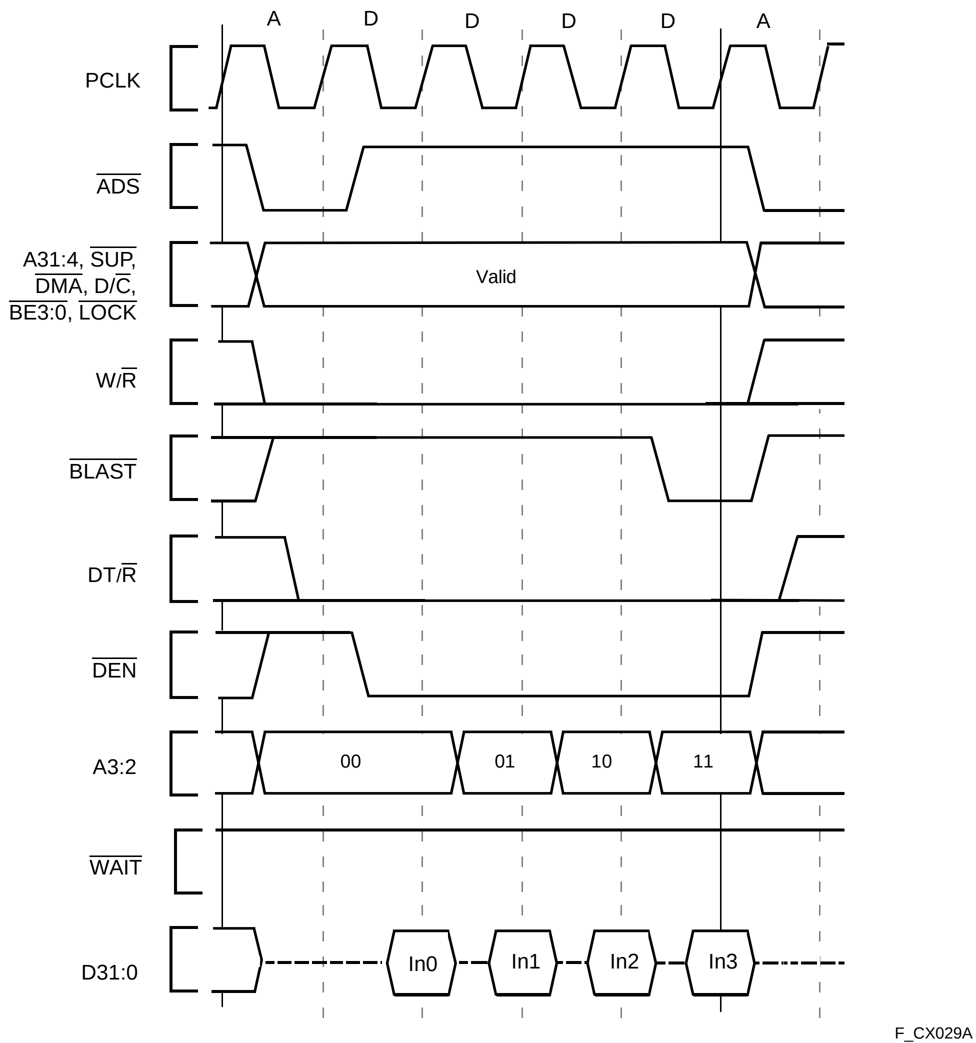


Figure 26. Burst, Non-Pipelined Read Request Without Wait States, 32-Bit Bus

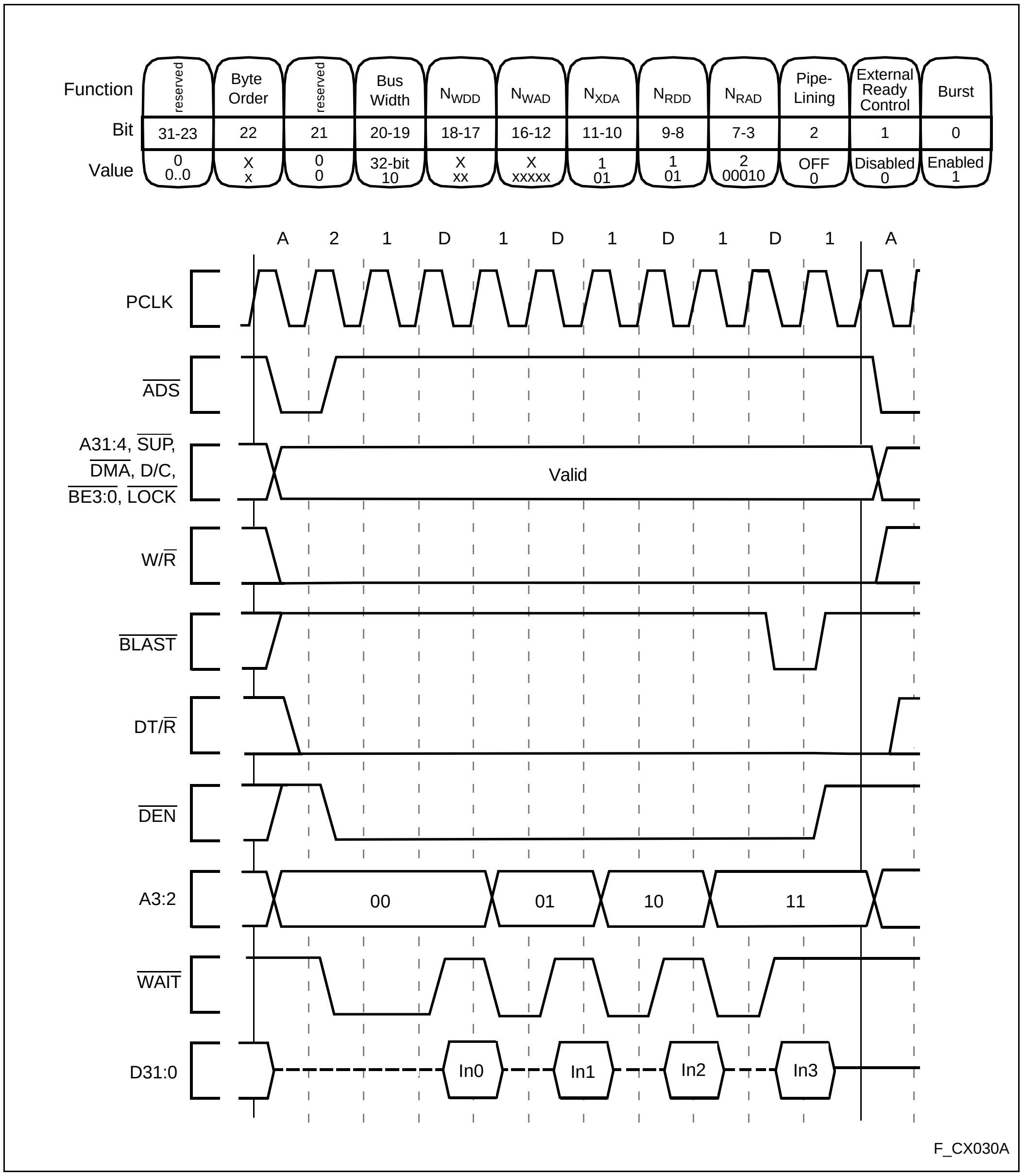


Figure 27. Burst, Non-Pipelined Read Request With Wait States, 32-Bit Bus

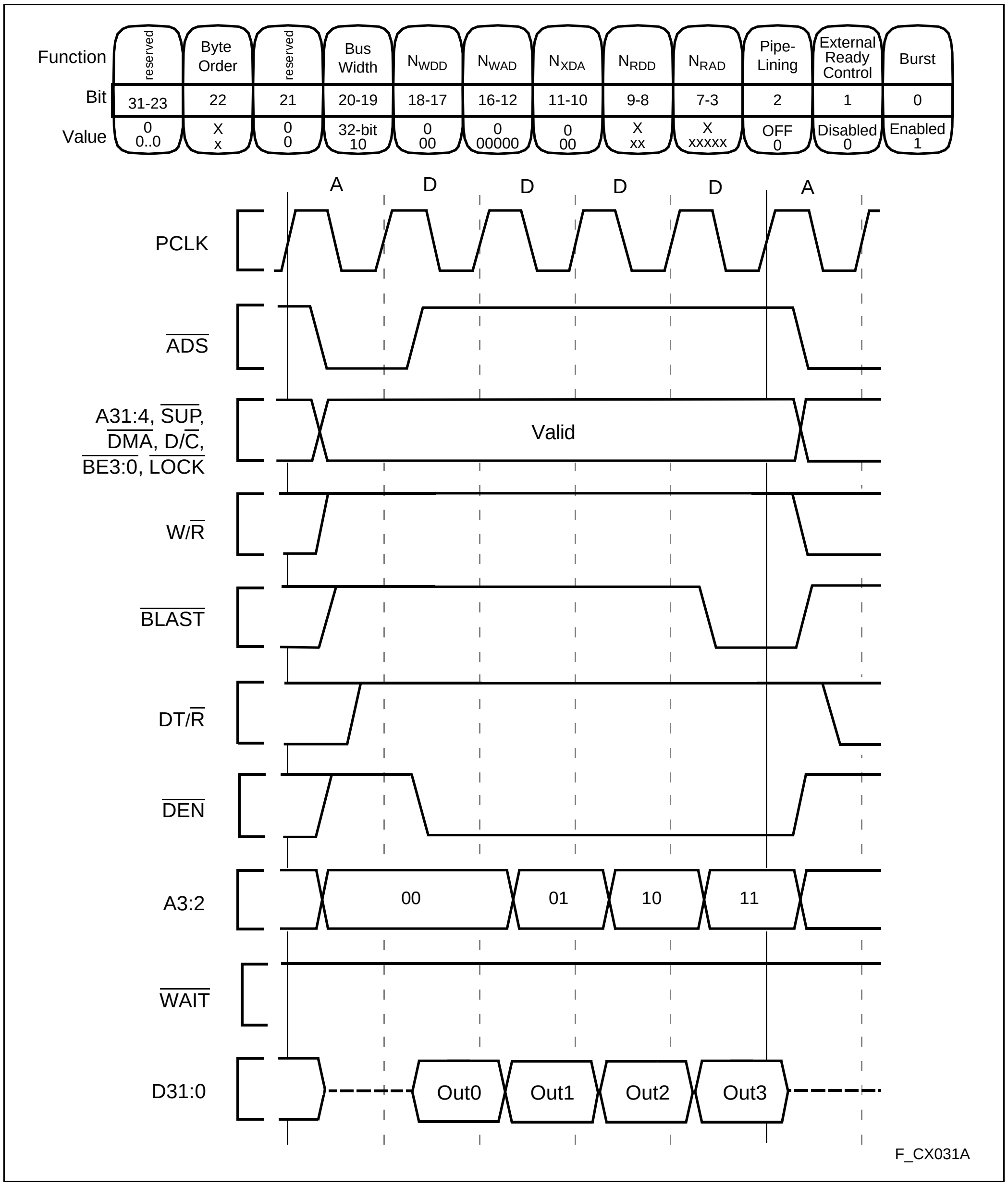


Figure 28. Burst, Non-Pipelined Write Request Without Wait States, 32-Bit Bus

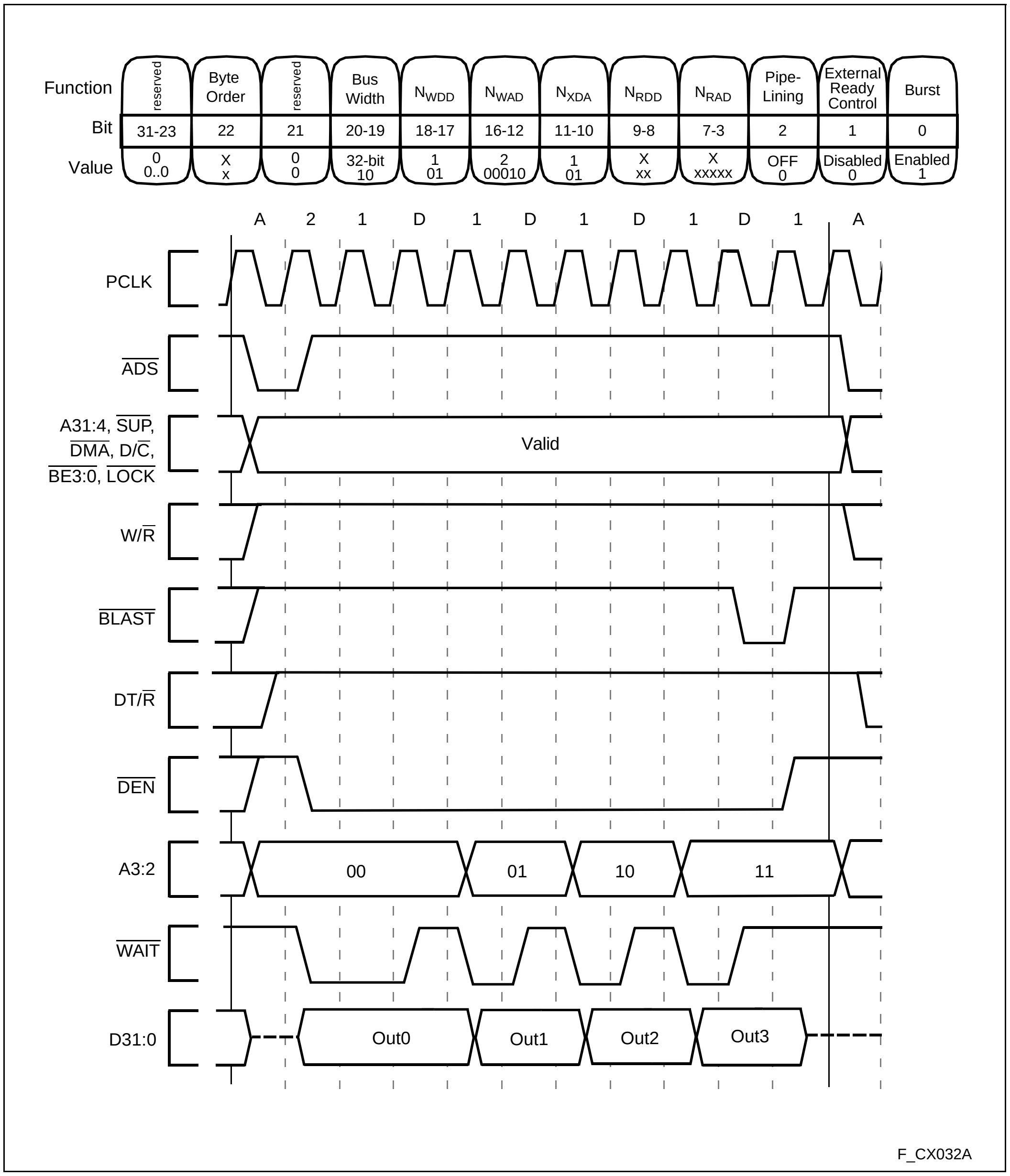


Figure 29. Burst, Non-Pipelined Write Request With Wait States, 32-Bit Bus

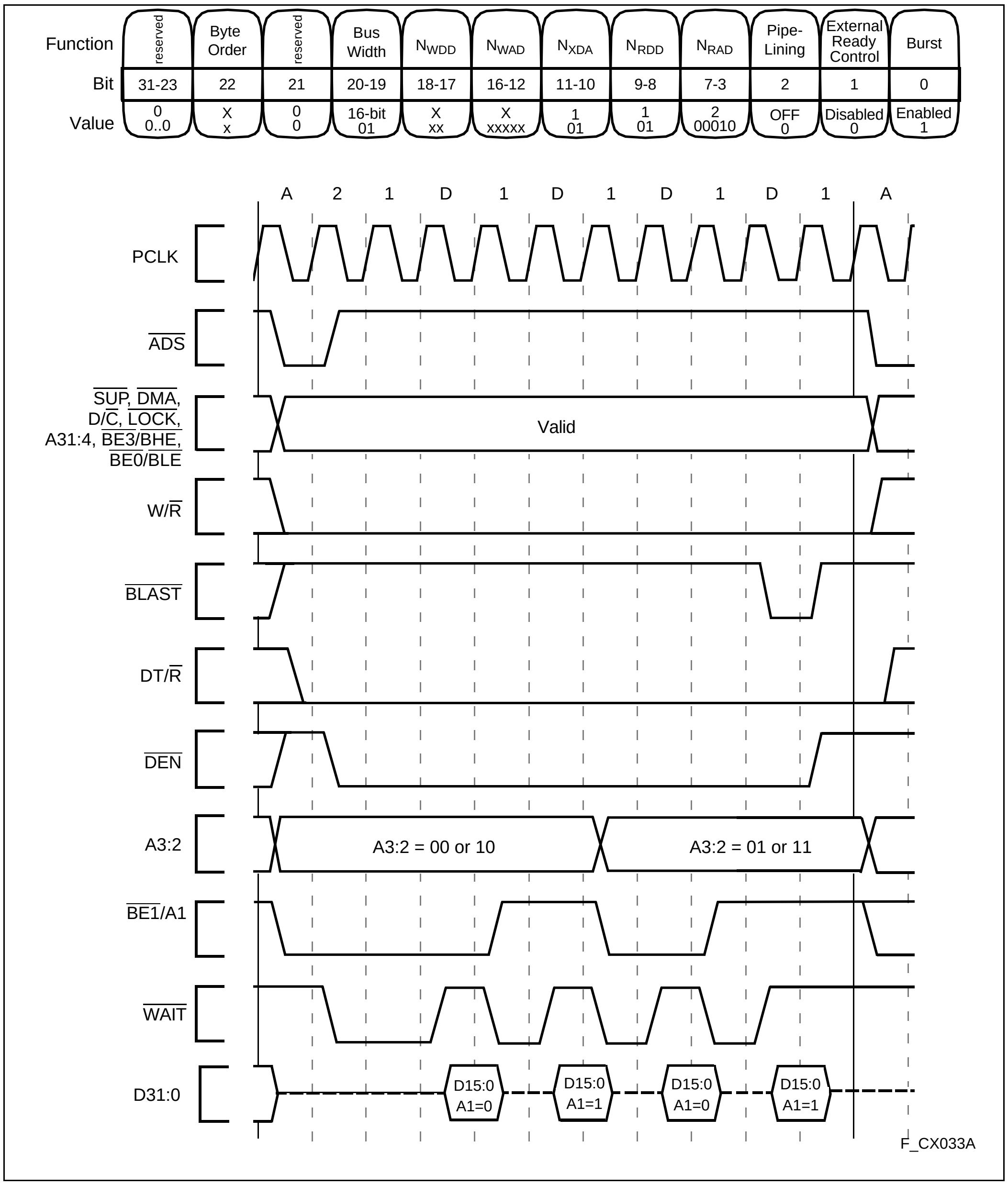


Figure 30. Burst, Non-Pipelined Read Request With Wait States, 16-Bit Bus

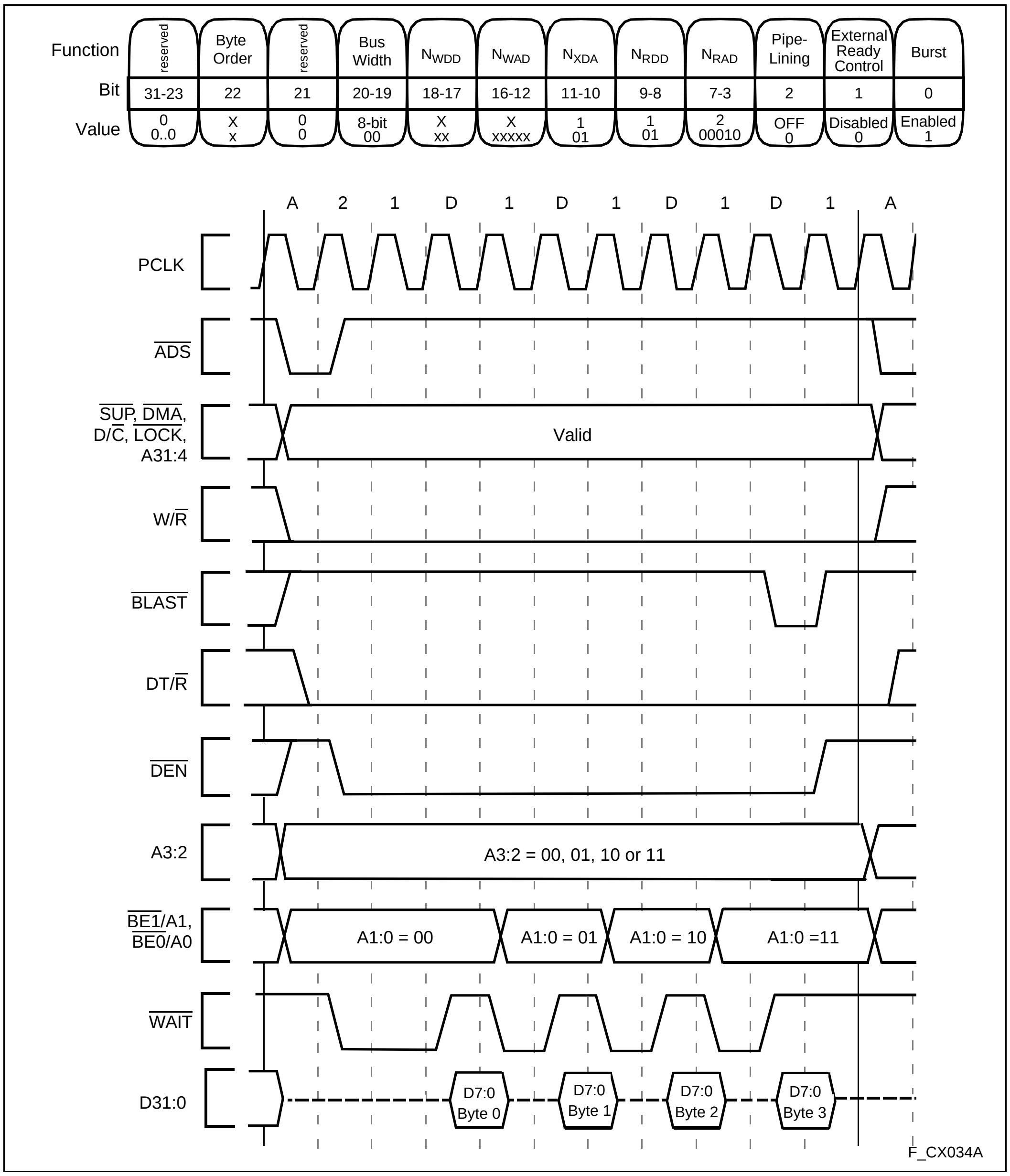


Figure 31. Burst, Non-Pipelined Read Request With Wait States, 8-Bit Bus

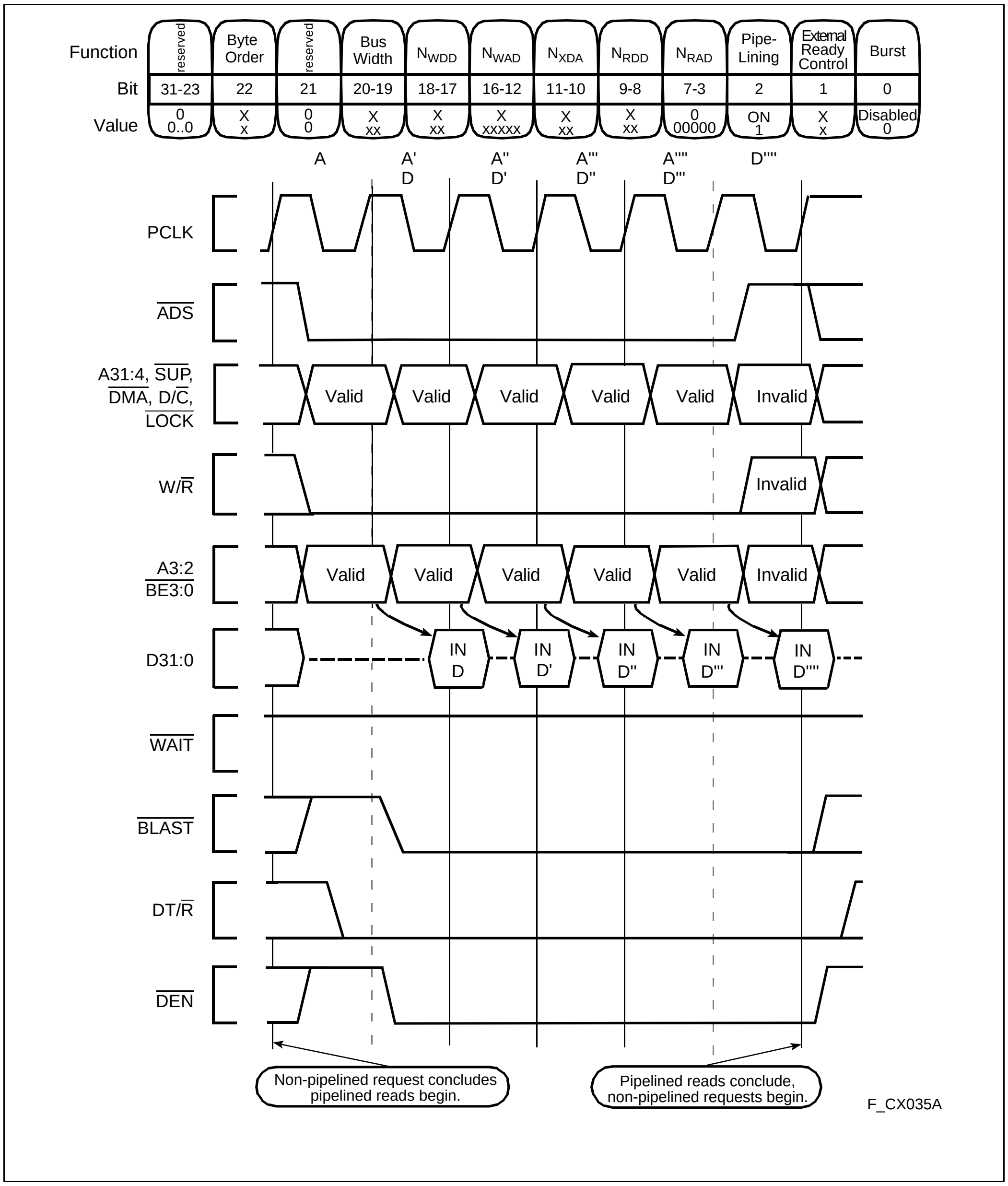


Figure 32. Non-Burst, Pipelined Read Request Without Wait States, 32-Bit Bus

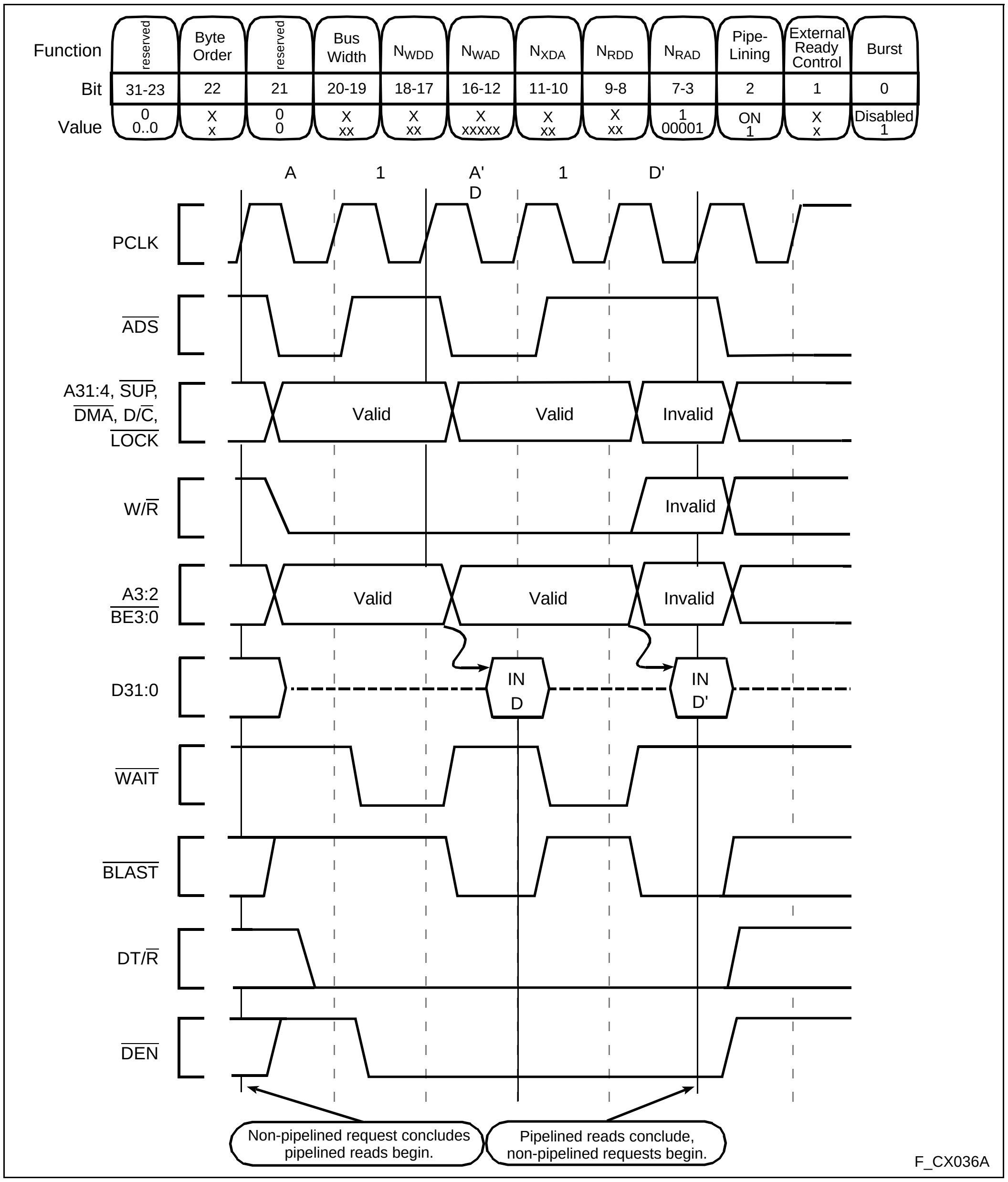


Figure 33. Non-Burst, Pipelined Read Request With Wait States, 32-Bit Bus

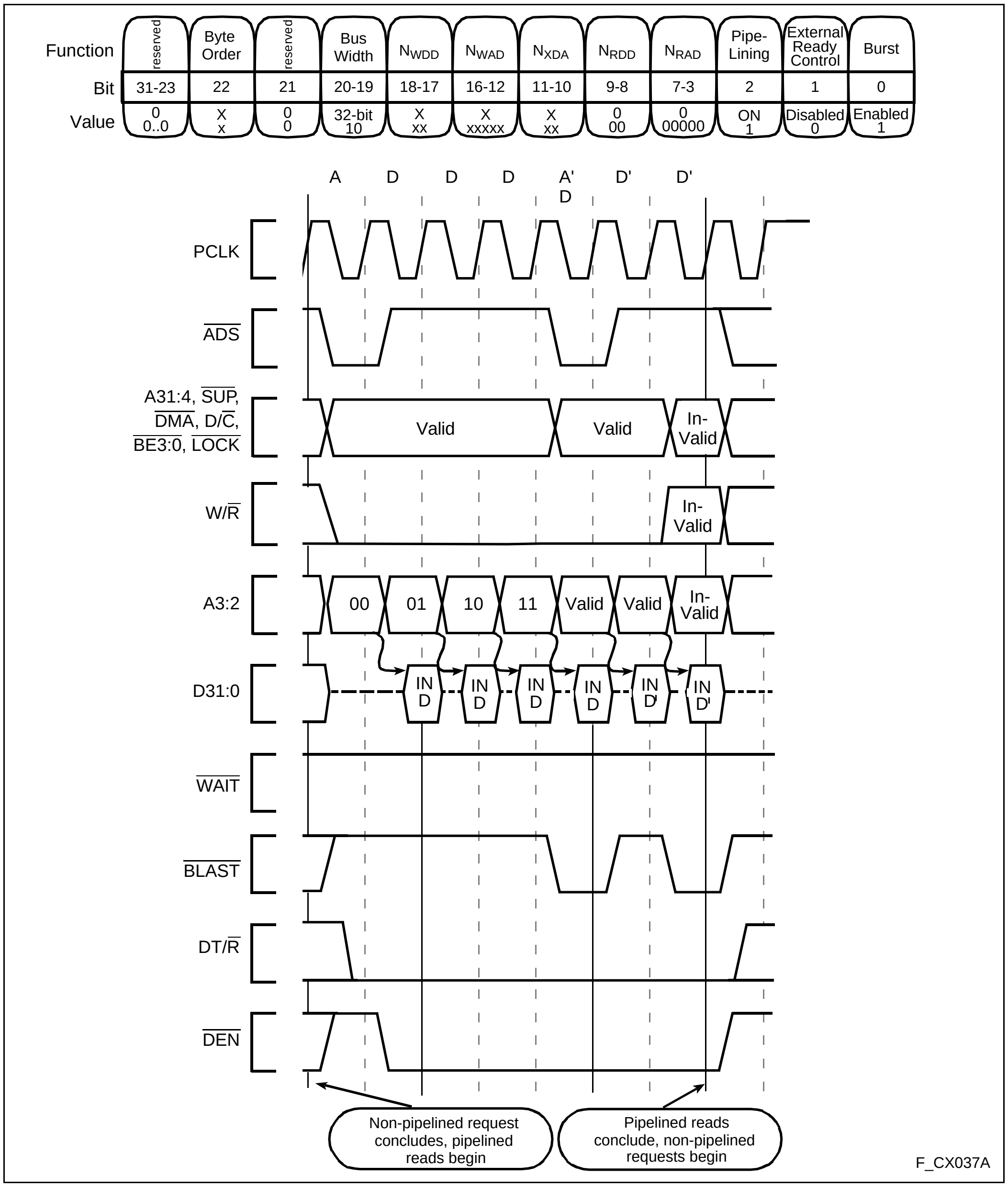


Figure 34. Burst, Pipelined Read Request Without Wait States, 32-Bit Bus

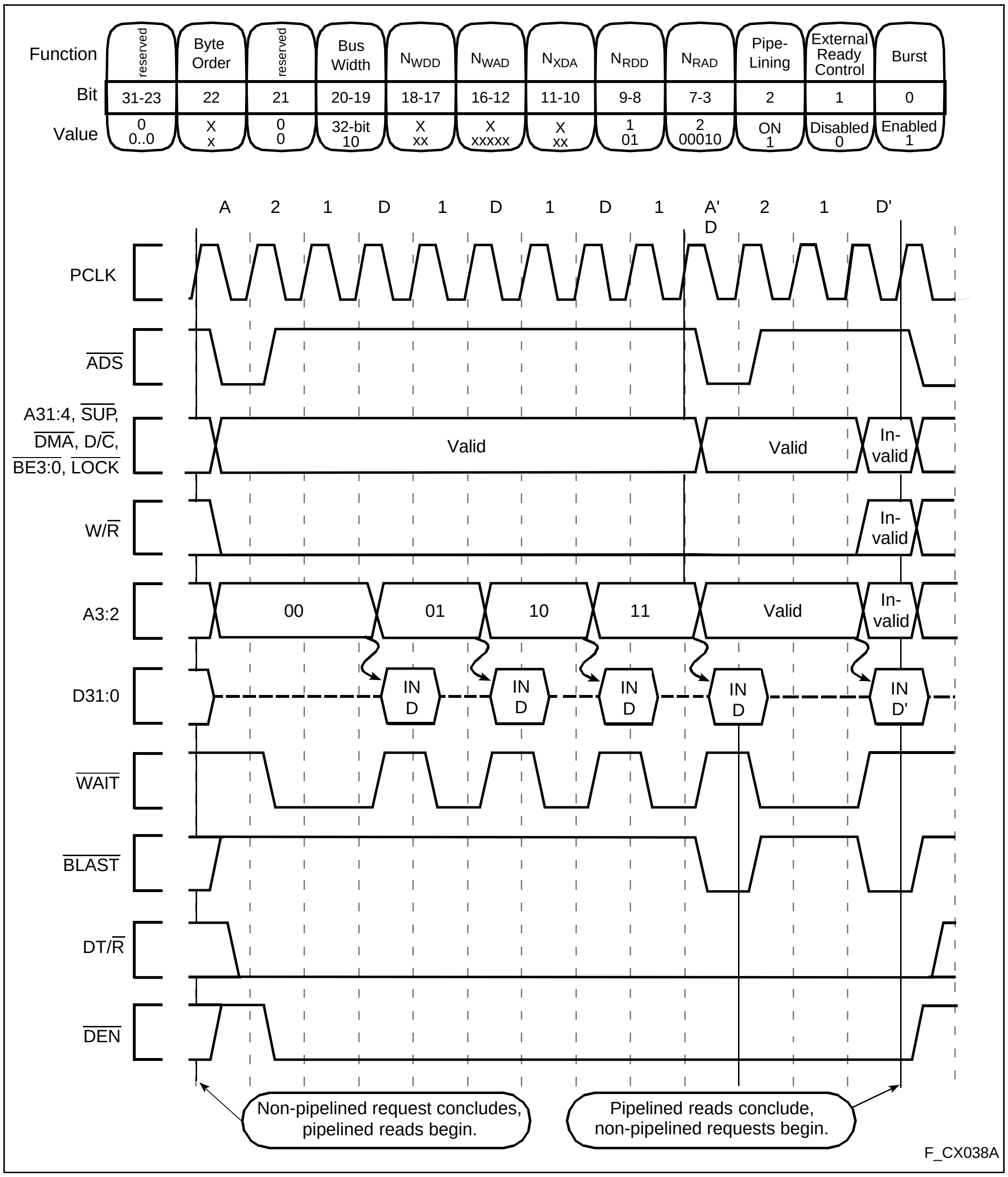


Figure 35. Burst, Pipelined Read Request With Wait States, 32-Bit Bus

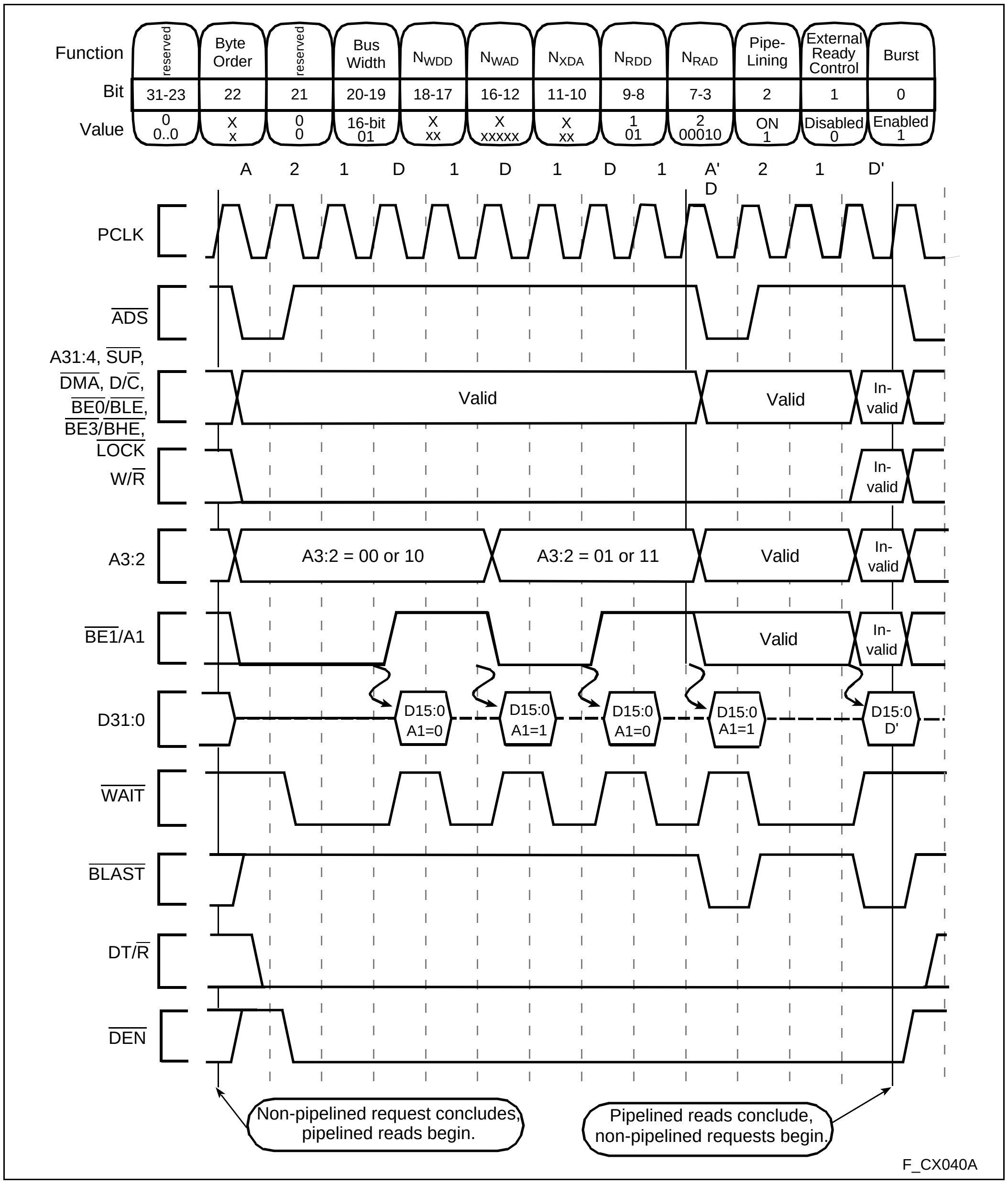


Figure 36. Burst, Pipelined Read Request With Wait States, 16-Bit Bus

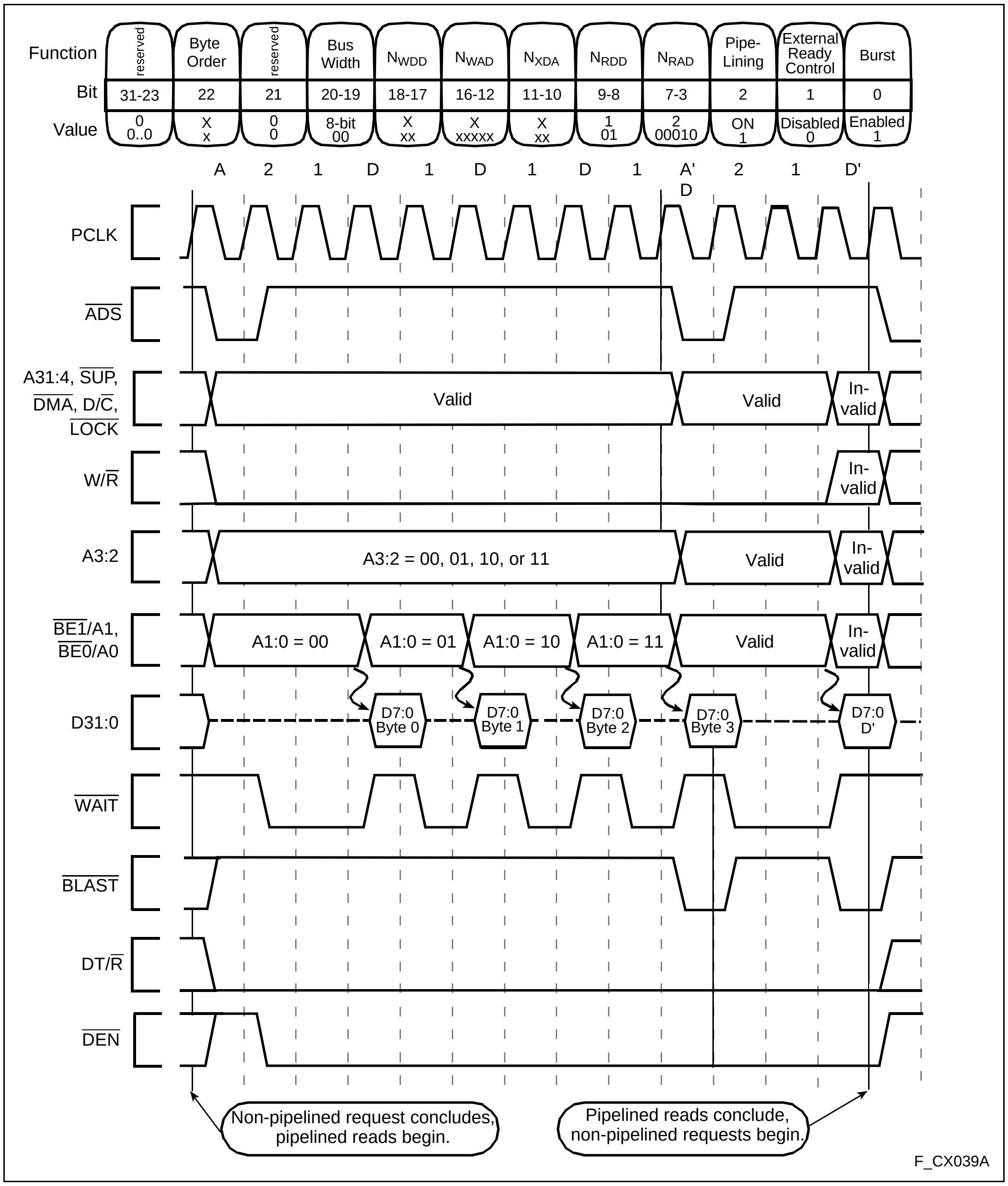


Figure 37. Burst, Pipelined Read Request With Wait States, 8-Bit Bus

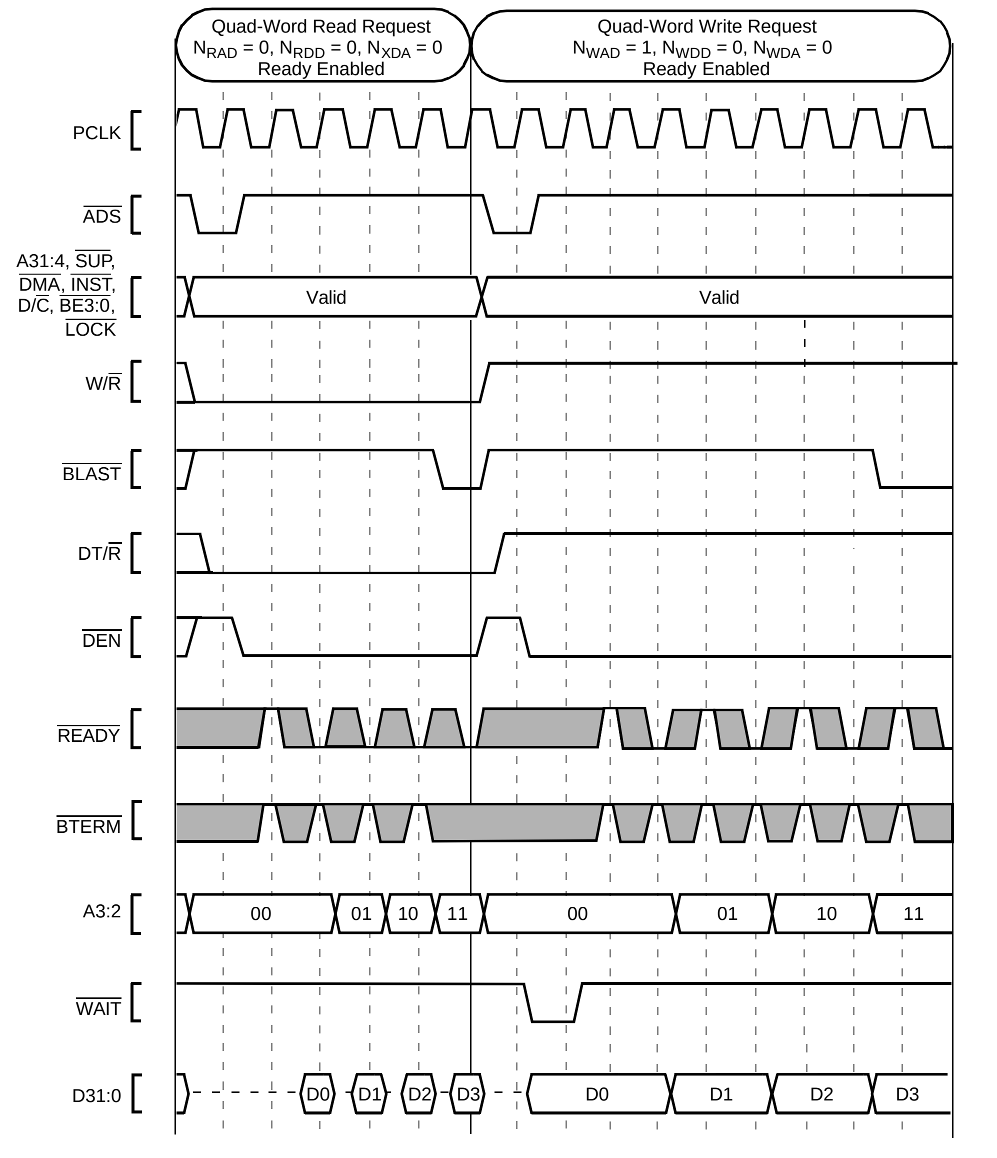
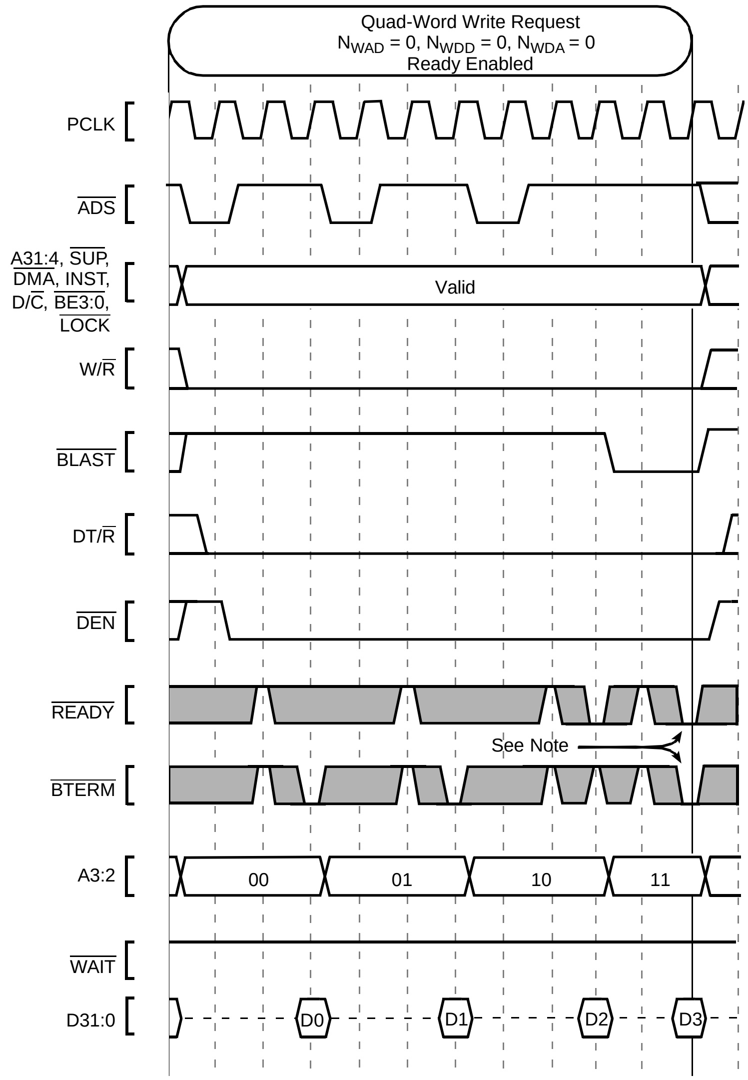


Figure 38. Using External READY



Note: READY adds memory access time to data transfers, whether or not the bus access is a burst access. BTERM interrupts a bus access, whether or not the bus access has more data transfers pending. Either the READY signal or the BTERM signal will terminate a bus access if the signal is asserted during the last (or only) data transfer of the bus access.

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Figure 39. Terminating a Burst with BTERM

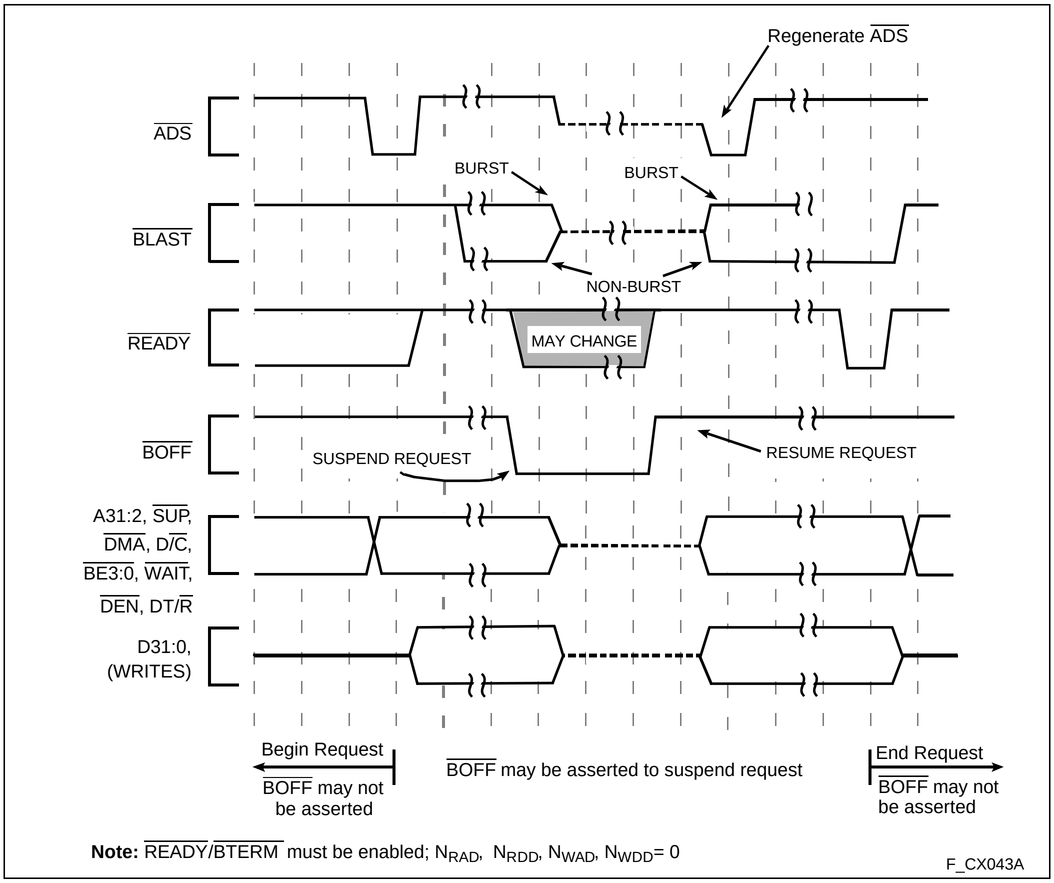


Figure 40. BOFF Functional Timing

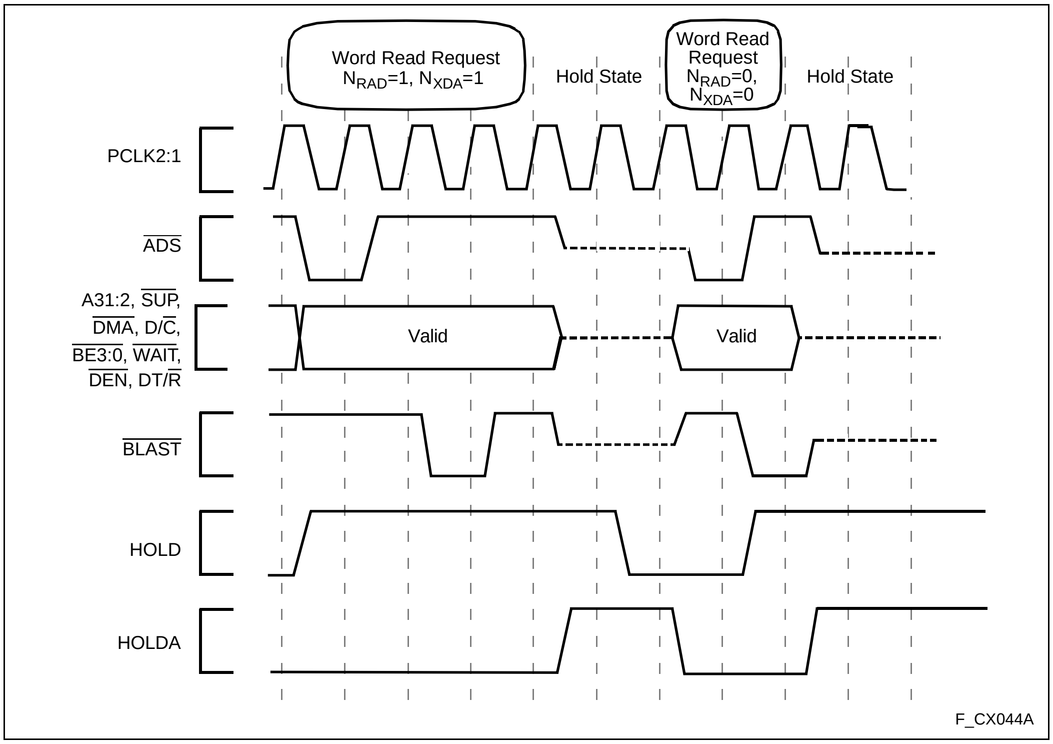
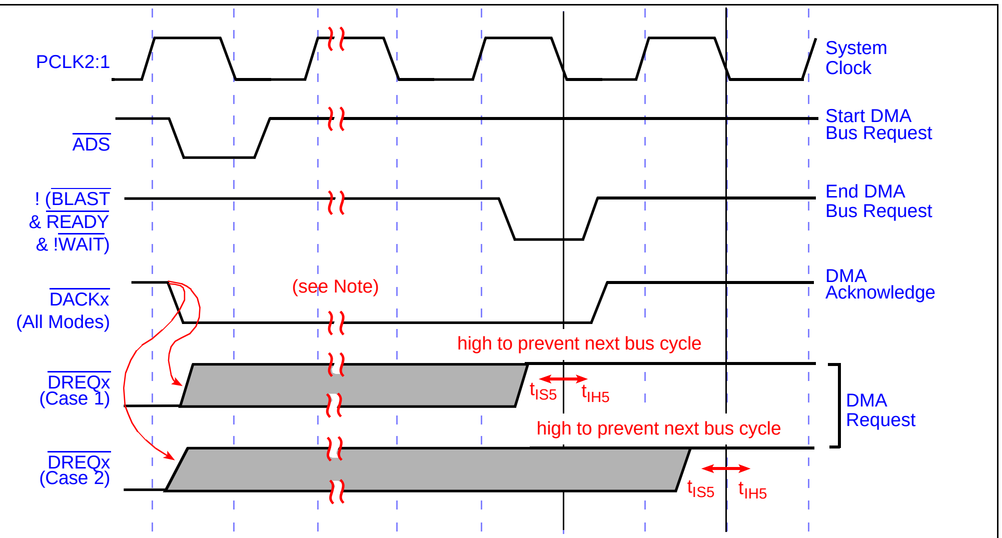


Figure 41. HOLD Functional Timing



Note:

1. Case 1: DREQ must deassert before DACK deasserts. This applies to all Fly-By modes: source synchronized packing modes and destination synchronized unpacking modes.
2. Case 2: DREQ must be deasserted by the second clock (rising edge) after DACK is driven high. This applies to all other DMA transfers.
3. DACKx is asserted for the duration of a DMA bus request. The request may consist of multiple bus accesses (defined by ADS and BLAST).

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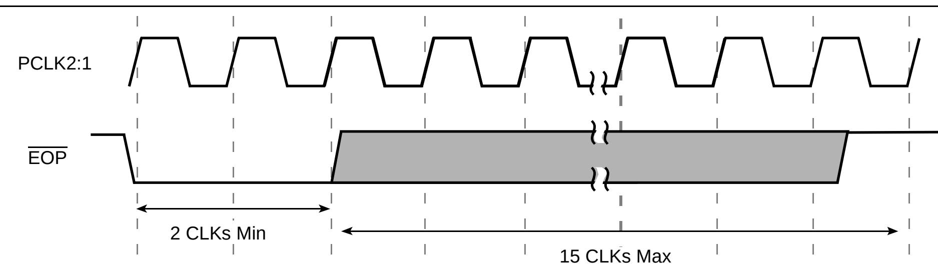
Figure 42. DREQ and DACK Functional Timing



Note: EOP has the same AC Timing Requirements as DREQ to prevent unwanted DMA requests. EOP is NOT edge triggered. EOP must be held for a minimum of 2 clock cycles then deasserted within 15 clock cycles.

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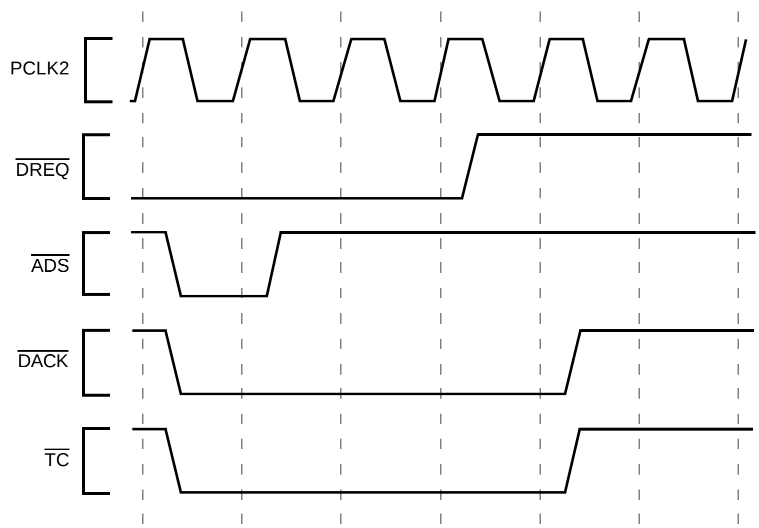
Figure 43. EOP Functional Timing



Note: Terminal Count becomes active during the last bus request of a buffer transfer. If the last LOAD/STORE bus request is executed as multiple bus accesses, the TC will be active for the entire bus request. Refer to the *i960® Cx Microprocessor User's Manual* for further information.

Figure 44. Terminal Count Functional Timing

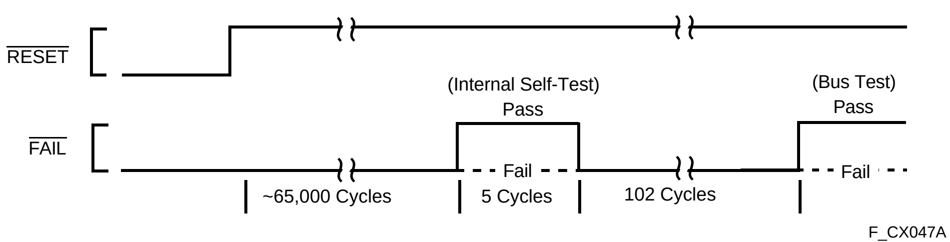


Figure 45. $\overline{\text{FAIL}}$ Functional Timing

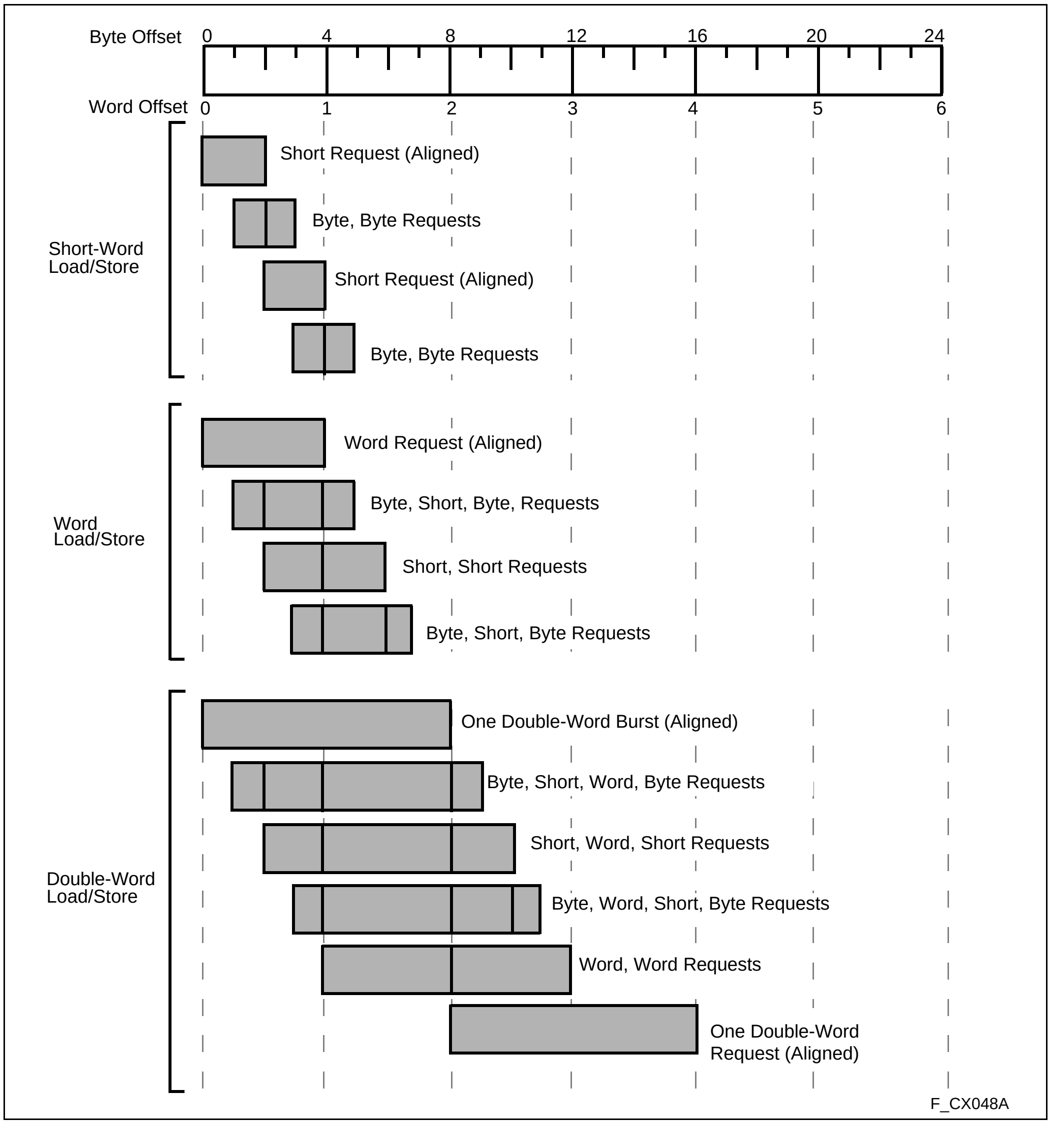


Figure 46. A Summary of Aligned and Unaligned Transfers for Little Endian Regions

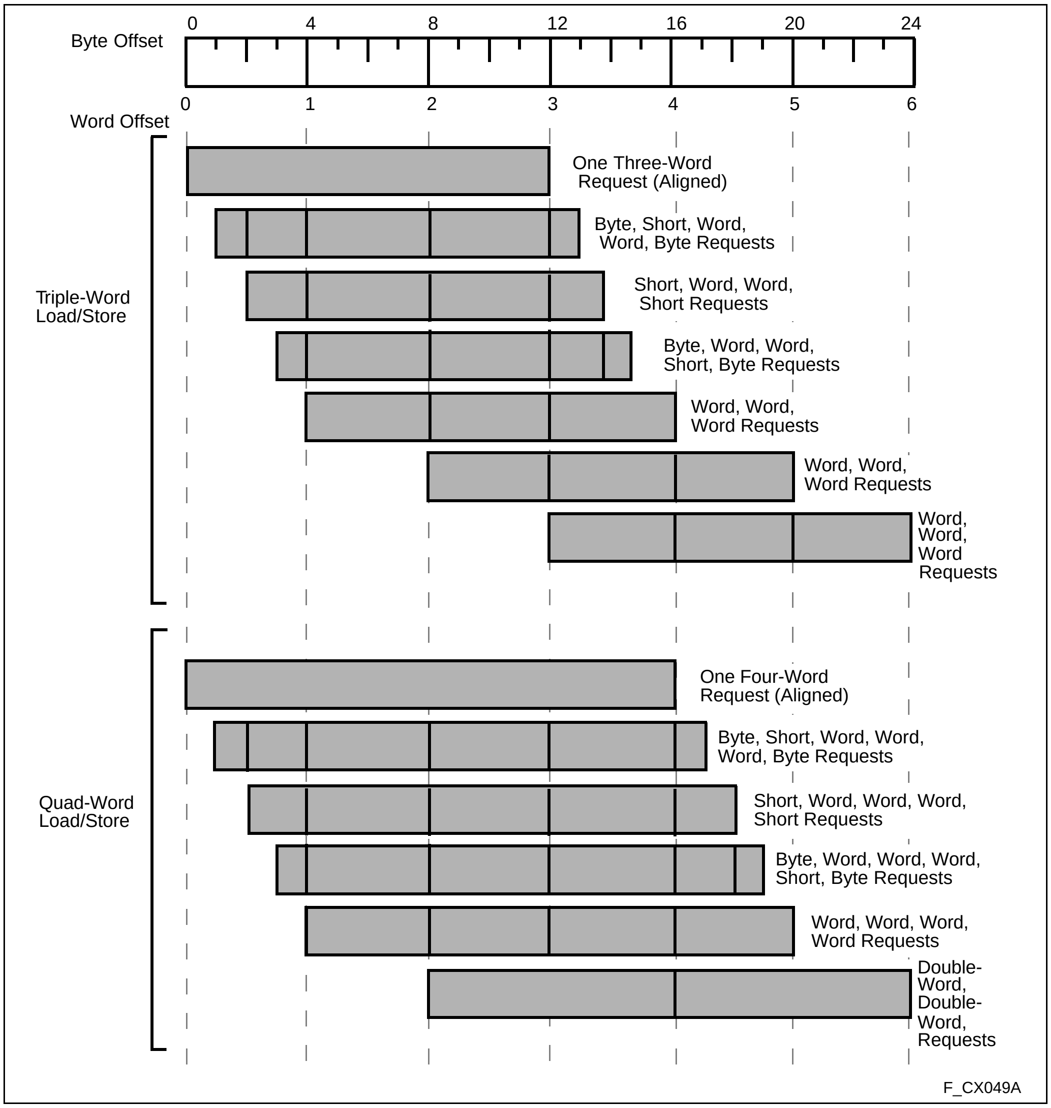


Figure 47. A Summary of Aligned and Unaligned Transfers for Little Endian Regions (Continued)

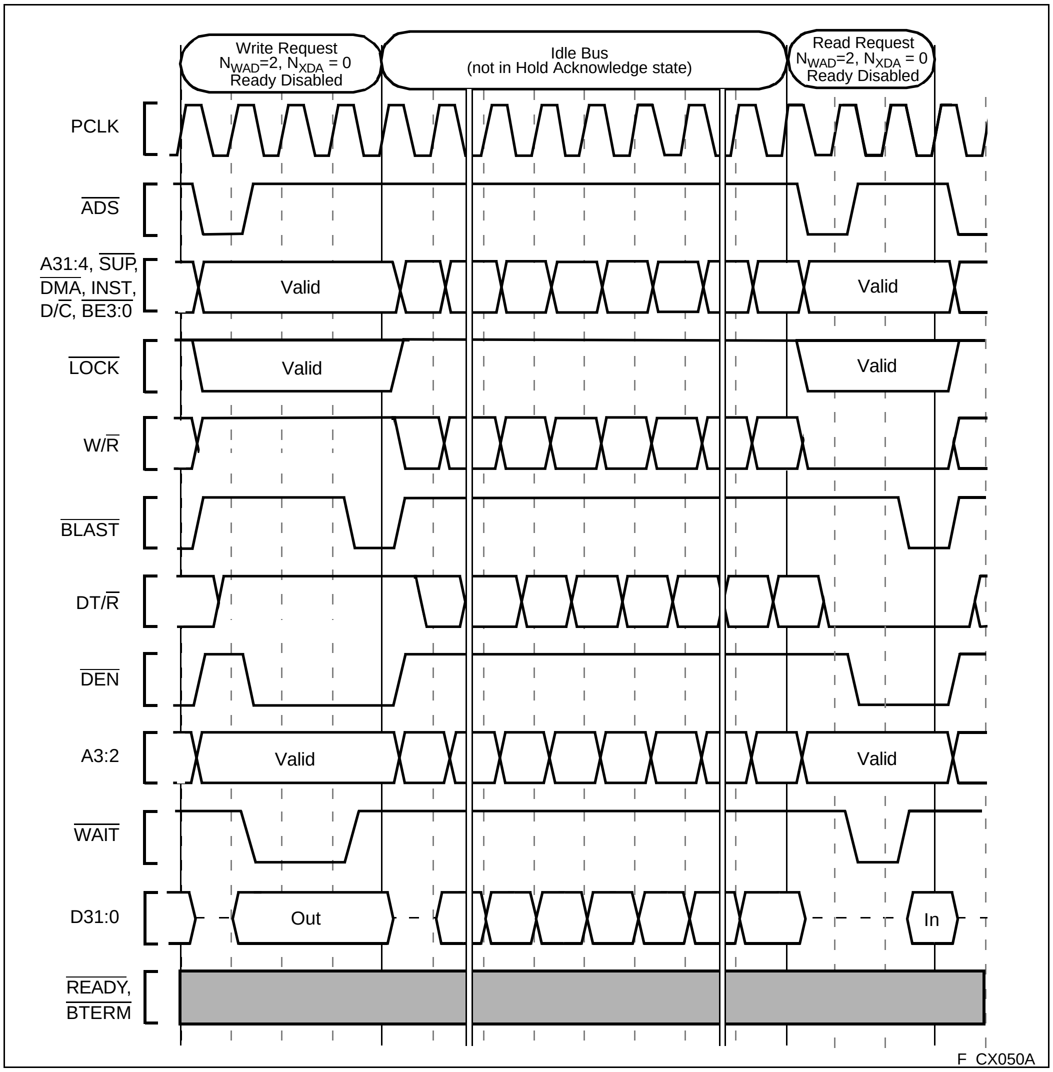


Figure 48. Idle Bus Operation

7.0 REVISION HISTORY

Section	Last Rev.	Description
Figure 15. Output Delay or Hold vs. Load Capacitance	-001	In the legend, the dashed line and the solid line were reversed.
Figure 17. ICC vs. Frequency and Temperature	-001	Tc tags were incorrectly reversed; T_C = 85° C should be TOP line

This is a new data sheet for the 80960CF-40 product. It is derived from the 80960CF-33, -25, -16 data sheet. Aside from a few minor edits, only the AC Characteristics differ from the 80960CF-33, -25, -16 data sheet.